ELECTROMIGRATION-DEPENDENT PARAMETRIC YIELD ESTIMATION

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ABSTRACT

We define and investigate the problem of electromigration faults caused by spot defects during VLSI manufacturing process. Analysis is given for a simple layout, and simulations are presented and discussed for a more complicated case. It is shown that in some cases, electromigration-dependent parametric faults can make a significant contribution to the total yield estimation.

1. INTRODUCTION

The deep sub-micron technology in today's very large scale integration (VLSI) manufacturing demands a special care of controlling the cost. The critical area of VLSI layout is a measure that reflects the sensitivity of the layout to defects occurring during the manufacturing process, and is widely used to predict the yield of a VLSI chip. The critical area is traditionally defined as the area of the region of the circuit layout in which the center of an average spot defect with typical properties has to fall in order to generate a circuit fault [1]. Recently, very effective ways of critical area estimation have been developed [2]. Still, critical area is only one of the methods to predict the yield of a chip. Other methods include statistical analysis using Monte-Carlo algorithms [3].

While yield estimation methods are quite different, they all aim to answer one question: "How many chips would be operational out of some produced amount?". The term *operational* usually corresponds to the catastrophic yield, meaning the chip fully complies to all logical specifications. Wagner and Koren in [4] discuss the *parametric yield*, in which the question is: "How many chips will have an acceptable performance?". The term *acceptable performance* may have different interpretations, e.g. frequency, power consumption, Mean Time To Failure (MTTF), supply voltage, ambient temperature, etc. In their paper they develop an approach to estimate the frequency dependant yield of long interconnect lines.

In this manuscript we shall focus on *electromigration-dependent parametric yield* (EPY), where one is concerned about the number of chips that will survive electromigration for a given period of time. In Section 2 the analytical treatment of EPY is presented; Section 3 deals with practical solution for finding EPY, and the Summary in Section 4 briefly recapitulates the main points of this research.

2. ANALYSIS

The probability of spatial defect depends on its location and size. Figures 1 and 2 show a pattern consisting of a single metal wire of width w much less than its length Y, deposited on an insulating substrate of width X. An imperfection in photo mask or photoresist, or contamination can result in the wire be partially or completely broken. If the wire is completely broken, such defect is called *fatal*, and is well studied [5]. In this section we study defects that cause a partially broken pattern, and calculate $f(w)$, the MTTF of a single wire. Among other deficiencies wire width reduction causes growth of current density, which, in turn, leads to MTTF degradation due to electromigration.

Let w_{req} be the minimal width of wire, such that for a given constant current, its MTTF is at least τ. For a defect to become *MTTF-parametric fault* with parameter τ, it should fall so that the remaining part of the wire has the width at most w_{req}.

We answer the following question: Where are the loci of defects that cause the MTTF-parametric fault with parameter τ? Answering the question requires considering two alternative cases, which are presented in Sec. 2.3 and 2.4. Sec. 2.1 and 2.2 give a required background.

2.1. Defects size distribution

The defect size probability distribution $S(r)$ is well-studied during last three decades. It is accepted to be

$$S(r) = \begin{cases} c_q r^q & 0 \le r \le r_0; \\ c_p r^{-p} & r_0 \le r \le r_M, \end{cases} \tag{1}$$

where r_0 is the defect radius at which the density function peaks, r_M is the maximum size defect expected to occur, $q \approx 1$, $p \approx 3$, c_q and c_p are constants such that $S(r)$ is continuous at r_0 and $\int_0^{r_M} S(r)dr = 1$ (see [6]).

It can be shown that for $r_0 \ll r_M$ (actually, for $r_M \to \infty$), $q = 1$, and $p = 3$

$$\begin{aligned} c_q &\approx \frac{1}{r_0^2} \\ c_p &\approx r_0^2. \end{aligned}$$

2.2. MTTF Versus Wire Width

Let us now calculate $f(w)$, the MTTF of a single wire of width w. Black in [7] develops the following equation:

$$\frac{wd}{MTTF} = AJ^2 e^{-\frac{\phi}{kT}},$$

where

w	wire width,
d	wire thickness,
$MTTF$	mean time to failure in the wire,
J	current density,
A	constant embodying physical metal properties,
ϕ	activation energy,
k	Boltzmann's constant,
T	wire temperature.

Assuming current I to be flowing through the wire, we get MTTF as a function of wire width provided all other parameters are constant:

$$\begin{aligned} MTTF = f(w) &= \frac{wd}{AJ^2 e^{-\frac{\phi}{kT}}} \\ &= \frac{wd}{A\frac{I^2}{w^2 d^2} e^{-\frac{\phi}{kT}}} \\ &= \left(\frac{d^3}{AI^2 e^{-\frac{\phi}{kT}}} \right) \cdot w^3. \end{aligned}$$

Defining

$$C \equiv \frac{d^3}{AI^2 e^{-\frac{\phi}{kT}}}$$

we get the following equation:

$$f(w) = C \cdot w^3. \qquad (3)$$

It would be useful to express the minimal width required for wire to survive at least t hours:

$$f^{-1}(t) = \sqrt[3]{t/C}. \qquad (4)$$

2.3. Small Defects

In this subsection we deal with relatively small radii of defects, $r \leq \frac{W}{2}$. Let L be the critical interval within which the defect must fall in order to cause a parametric fault, i.e., the wire would be operational, but is expected to fail after some time τ due to electromigration. L designates the length of the loci of defects

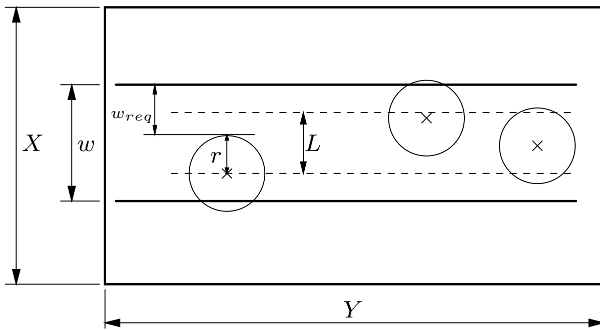

Figure 1: A single wire of width w in the die of size X; with 3 defects of radius r. The critical interval will be a single strip only if $r \leq \frac{w}{2}$.

centers that cause the desired MTTF reduction to at most τ, while $w_{req} = f^{-1}(\tau)$.

Summation of lengths leads to the following equations:

$$\begin{aligned} w &= w_{req} + r + \frac{w - L}{2} \\ L &= 2w_{req} + 2r - w. \end{aligned}$$

The MTTF-parametric fault with radius r will appear with probability equal to the ratio of L to the total width X on which the fault can fall.

$$prob_1(t \leq \tau \mid r) = \frac{2f^{-1}(\tau) + 2r - w}{X}$$

As said, the wire's remaining width should be at least $w_{req} = f^{-1}(\tau)$. Therefore the defects with radius less then $\frac{w - w_{req}}{2}$ do not contribute MTTF-parametric fault. The *average electromigration-dependent parametric fault probability* (or EP fault probability) for all defects may be obtained by integrating $prob_1$ multiplied by the fractional number of defects with radius r over radii sizes

$$prob_1(t \leq \tau) = \int_{\frac{w - f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau) + 2r - w}{X} \cdot S(r)dr. \qquad (6)$$

2.4. Big Defects

Now we have to treat another case, where the defect's radius is grater then half the wire's width ($r \geq \frac{w}{2}$). In this case, the critical area, in which the defect must fall in order to cause parametric fault but not catastrophic fault, is built up of two strips each one of height w_{req} (see Figure 2).

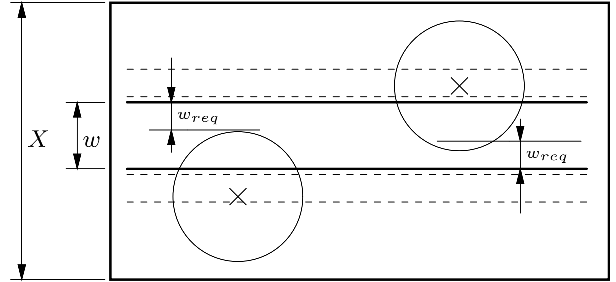

Figure 2: Two defects grater then wire width w. The critical interval is split into two strips.

Therefore we get

$$\begin{aligned} L &= 2w_{req} \\ prob_2(t \leq \tau \mid r) &= \frac{2f^{-1}(\tau)}{X}, \end{aligned}$$

and finally

$$prob_2(t \leq \tau) = \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau)}{X} \cdot S(r)dr. \qquad (7)$$

Actually, the upper limit of integration in the last equation should be finite, since defect size is bounded by the die size. Eq. 1 shows that the likelihood of defects bigger than die is very small, therefore we disregard them. Details regarding bounded and unbounded critical area may be found in [8].

2.5. Average Electromigration-dependent Parametric Fault Probability

Since the Equations 6 and 7 are mutually exclusive, the total probability is the sum of the two probabilities:

$$prob(t \le \tau) = prob_1(t \le \tau) + prob_2(t \le \tau). \quad (8)$$

As shown in Sec. 2.1, $S(r)$ is defined differently in two intervals. Hence, if $\frac{w}{2} \le r_0$,

$$prob(t \le \tau) = \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau)+2r-w}{X} \cdot c_q r dr + + \int_{\frac{w}{2}}^{r_0} \frac{2f^{-1}(\tau)}{X} \cdot c_q r dr + + \int_{r_0}^{\infty} \frac{2f^{-1}(\tau)}{X} \cdot \frac{c_p}{r^3} dr,$$

which for $c_q = 1/r_0^2$, $c_p = r_0^2$ yields

$$prob(t \le \tau) = \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{2f^{-1}(\tau)+2r-w}{Xr_0^2} r dr + + \int_{\frac{w}{2}}^{r_0} \frac{2f^{-1}(\tau) r dr}{Xr_0^2} dr + \int_{r_0}^{\infty} \frac{2f^{-1}(\tau) r_0^2}{Xr^3} dr$$

$$prob(t \le \tau) = \frac{f^{-1}(\tau)(9wf^{-1}(\tau) + 48r_0^2 - 4f^{-1}(\tau)^2 - 6w^2)}{24Xr_0^2}. \quad (9)$$

When $\frac{w}{2} \ge r_0$, we shall examine two cases: $r_0 \ge \frac{w-f^{-1}(\tau)}{2}$ and $r_0 \le \frac{w-f^{-1}(\tau)}{2}$. Thus

$$prob(t \le \tau \,|_{r_0 \ge \frac{w-f^{-1}(\tau)}{2}}) = = \int_{\frac{w-f^{-1}(\tau)}{2}}^{r_0} \frac{(2f^{-1}(\tau)+2r-w)r}{Xr_0^2} dr + + \int_{r_0}^{\frac{w}{2}} \frac{(2f^{-1}(\tau)+2r-w)r_0^2}{Xr^3} dr + \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau) r_0^2}{Xr^3} dr$$

$$prob_{2a}(t \le \tau \,|_{r_0 \ge \frac{w-f^{-1}(\tau)}{2}}) = = \frac{64wr_0^3 + w^4 - 6w^3 f^{-1}(\tau) + 9w^2(f^{-1}(\tau))^2}{24wXr_0^2} + + \frac{48wf^{-1}(\tau)r_0^2 - 4w(f^{-1}(\tau))^3 - 24w^2r_0^2 - 48r_0^4}{24wXr_0^2}. \quad (10)$$

$$prob(t \le \tau \,|_{r_0 \le \frac{w-f^{-1}(\tau)}{2}}) = = \int_{\frac{w-f^{-1}(\tau)}{2}}^{\frac{w}{2}} \frac{(2f^{-1}(\tau)+2r-w)r_0^2}{Xr^3} dr + \int_{\frac{w}{2}}^{\infty} \frac{2f^{-1}(\tau) r_0^2}{Xr^3} dr$$

$$prob(t \le \tau \,|_{r_0 \le \frac{w-f^{-1}(\tau)}{2}}) = \frac{2f^{-1}(\tau) r_0^2 (2w - f^{-1}(\tau))}{wX(f^{-1}(\tau) - w)^2} \quad (11)$$

Summarizing the preceding results, note that Eq. 9, 10, and 11 refer to three different cases of relations between r_0, τ, and w. Also, recall that from Eq. 4, $f^{-1}(\tau) = \sqrt[3]{\tau/C}$.

All the above results have an apparent property: when the required width decreases towards zero, meaning the DC current in the wire is negligibly small, the average EP fault probability tends towards zero too. Indeed, Equations 9 and 11 have w_{req} as a factor in the numerator, causing the whole expression to go to zero. Equation 10, however, is not feasible under the assumption $w_{req} \to 0$, since its two conditions $r_0 > \frac{w-w_{req}}{2} = \frac{w}{2}$ and $\frac{w}{2} \ge r_0$ become contradictory.

Thereby, the EPY is more meaningful for nets with DC currents, such as power grid wires and analog circuits with strong bias current.

3. SIMULATIONS

The analysis in the previous section shows how complicated is the analytical solution for even very simple structure. For realistic patterns the analytical treatment becomes much more complicated because the figures do not have the same shape and size, and usually do not have a simple periodicity.

The analytical treatment, such as that shown in Section 2, helps to understand the concepts more promptly, but simulation is needed to determine the EP fault probability for realistic layout configurations. This section describes our simulations for estimating the extent of the EPY in a number of cases.

The simulator generates random defects with radius that obeys the rules described in Sec. 2.1, in a uniformly distributed position, and places it upon chip layout. If an event of catastrophic or parametric fault occurs, it is recorded. This process is repeated a large number of times (1000 to 10000). After that the statistics are output. The EPYSIM simulator is our implementation of EPY simulator. It has been written in C++ and contains about 1400 lines of code. EPYSIM was used firstly to simulate single metal wire pattern used in Section 2 in order to ensure its validity. Figure 3 shows the simulation results and analytical solution for EP fault probability as a function of the current in the wire, showing quite a good matching with analytical solution. Secondly, the simulator

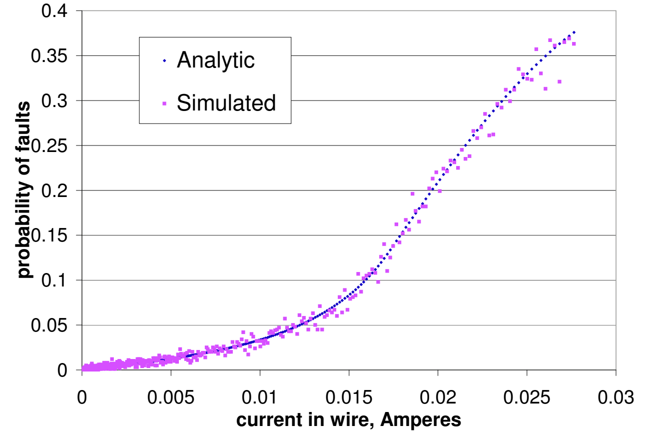

Figure 3: The simulated and analytically calculated MTTF-dependent parametric fault probability as a function of current in a single wire.

was run on real design. The design was a NAND2 gate, drawn in Cadence, compiled, and brought to layout (see Fig. 4). Then a circuit was extracted from the layout and simulated using Spectre

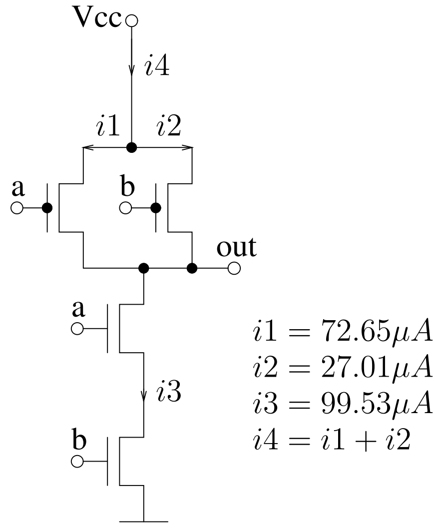

Figure 4: The NAND gate used for simulations and average DC currents in the branches. Only DC component of the current affects MTTF due to electromigration, as described in [9].

to get currents in wires. Then the layout (in CIF format) along with currents data was supplied to EPYSIM. A scrupulous analysis applied to extract the DC components in the branches within the gate.

Simulation result of interest is a plot of the ratio of the number of parametric faults to the number of catastrophic faults for different given MTTFs, see Fig. 5. This comparison to catastrophic

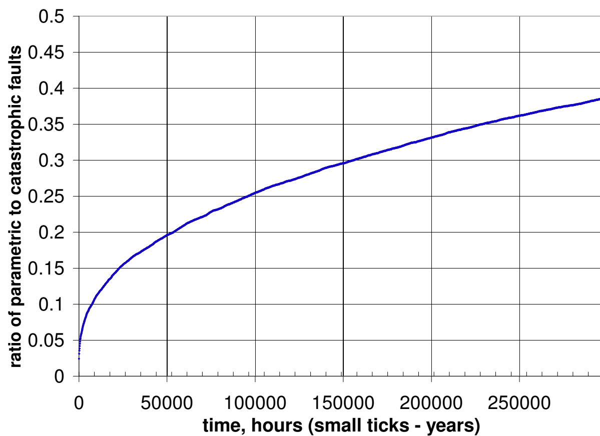

Figure 5: The simulation of NAND gate presented in Fig. 4 under the temperature of 400°K. The graph shows that the effect of EPY may be large.

yield gives the insight on the influence of the EPY on the chip. For example, Figure 5 shows that for given conditions the overall yield is reduced by 20% after 6 years. This demonstrates that even for small digital circuits the contribution of EPY is not negligible. We believe that in chips with strong DC currents, like high-power digital circuits, some analog circuits, etc. the effect will be even stronger.

4. SUMMARY

In this paper a new yield problem is defined: what is the measure of non-catastrophic chip faults due to electromigration as a result of defects at fabrication stage? Analysis was presented for a simple case of a single wire in the center of large die. The electromigration-dependent parametric fault probability of this pattern is a multicased expression that depends on about 10 parameters. A special simulation program — EPYSIM — was used to compare the analytical calculations with real defects, and to observe the EPY on more complicated patterns, as NAND gate. We show that in some cases the EPY makes a significant contribution to yield estimation of VLSI chip.

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