Professor Avi (Abraham) Mendelson

CURRICULUM VITAE

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1 Personal Details

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2 Higher Education

A. Undergraduate and Graduate Studies

Period of Study	Name of Institution and Department	Degree	Year of Approval of Degree
1987—1990	Electrical Engineering Department, University of Massachusetts at Amherst	Ph.D	1990
1980 -1982	Computer Science Department, Technion	.MSC	1982
1975—1979	Computer Science Department, Technion	BSC	1979

3 Academic Ranks and Tenure in Institutes of Higher Education

Dates	Name of Institution and Department	Rank/Position
2016	EE Department, NTU University (Singapore)	Visiting (Full) Professor
2015 - Current	Kinneret Collage	Professor (full), head of the EE department.
2011 - Current	Technion -- EE and CS departments	Visiting (full) professor
2004 - 2011	Technion -- EE and CS departments	Adjunct Senior Teaching Fellow
2000 - 2004	Technion -- EE and CS departments	Adjunct Senior Lecturer
1998 - 1999	Technion -- EE department	Adjunct Lecturer
1991 - 1998	Technion -- EE department	Lecturer

4 Offices in Academic Administration

2011 – 2016 Head of the Nvidia Center of Education (together with Prof Mark Silberstein), Technion

2011 – Current Member of the Parallel System Lab. In both CS and EE departments, Technion

1994 – 1998 Head of the Parallel system Lab, EE Department, Technion

5 Scholarly Positions and Activities outside the Institution

5.1 Membership:

- IEEE Fellow
- ACM, IEEE, IEEE-Computer society

5.2 Editorial:

- 2014 – Current Associate Editor, IEEE Transactions on Computers

- 2010 – 2014 Associate Editor, IEEE Computer Architecture Letters (finished a full term)

5.3 Award committees and special committees

- 2017 – 2019 IEEE Computer Society Board of Governor
- 2017 – Current Chair of the Eckert-Mauchly awards committee (the most prestigious award for computer architect)
- 2015 – 2017 Member of the Eckert-Mauchly awards committee
- 2013 – Current Member of the Computer Science Advisory board of the Ministry of Education, Israel
- 2013 – Current Member of the CECL (manage the ACM chapter activities in Europe)
- 2013 – 2014 Head of the ACM distinguished member committee (together with Prof. Lorry Clark)
- 2010 – 2014 Member of the ACM distinguished member committee
- 2009 - 2014 Member of the ACM-Europe Council (full term)

5.4 Advisory Boards (Academic)

- 2013 – 2017 Advisory board of ISCA conference (the main conference for Computer Architecture)
- 2008 – 2013 Member of the advisory board of Microsoft Lab in BSC, Barcelona
- 2008 – 2016 Member of the industrial board of HiPEAC network of excellence

5.5 Referee:

Every year I am doing 20-30 paper reviews for leading Journals and conferences

5.6 Program Committee of major conferences

Participants in more than 30 program committees of major conferences, including

- International conference on Computer architecture (ISCA)
- Architecture that supports Programming languages and operating systems (ASPLOS)
- International conference on Microarchitectures (MICRO)
- International conference of parallel Architecture and compilers (PACT)
- High performance Embedded systems and architecture (HiPEAC)
- Parallel and Distributed Computing and Networks (PDCN).
- ACM international conference on Supercomputing (ICS)

5.7 Participation in Scholarly Conferences

(In this section I am providing only "samples" of the different talks, invited distinguished talk and similar activities I was part)

a. **Active Participation – Panelist, Keynote and invited talks**

International

Date	Name of Conference	Place of Conference	Subject of Lecture/Discussion	Role
2017	**IEEE AI/Machine Learning & Cybersecurity Confluence**	**Philadelphia, USA**	**AI/Machine Learning & Cybersecurity Confluence**	**By invite participation**
2016	**RoMoL**	**Barcelona**	Panel on the future of Runtime systems	**Panelist**
2015	**EMC^2**	**Viena**	Power managements in parallel embedded systems	**Invited talk**
2015	**Conf. on Medical devoces**	**China**	Innovation – Technology for the Society	**Invited talk**
2014	**SIAT institute**	**China**	The challenge of Fault-Tolerance mechanisms for power-efficient massive parallel systems	**Invited talk**
2014	**HiPEAC**	**Barcelona**	HiPEAC's impart on the Academic and Industry in Europe"	**Invited talk**
2014	**DAC Conf.**	**Germany**	GPGPU for dependable systems – a blessing or a curse?	**Keynote speech**
2013	International	**France**	The Challenge of Fault-	**Keynote**

	symposium on Computer Architecture and High Performance Computing		Tolerance Mechanisms for Power-efficient Massive Parallel Systems	**speech**
2013	ISCA	**Tel-Aviv**	Opening and Closing remarks for ISCA'2013	**Duty as a general chair**
2010	Multicore workshop	**Barcelona**	Will SW cope with the developing paste of parallel HW?	**Panelist and moderator**
2009	Distinguish lecture serious	**Illinois, USA**	Industrial and Research Challenges in the Area of Multi-Core and Many Cores	**Keynote speech**
2008	Date	**Germany**	Issues and Challenges in Dependable Embedded Systems	**Invited talk**
2007	ICS	**USA**	Multi-cores, many-cores and special cores	**Keynote speech**
2006	IMSS	**USA**	Memory management challenges in the power-aware computing era	**Keynote speech**

In Israel

Date	**Name of Conference**	**Place of Conference**	**Subject of Lecture/Discussion**	**Role**
2016	**Metro**	**Haifa**	Processing Real-time Streaming Data	**Invited talk**
2006	**IBM workshop**	**Haifa**	How many cores are too many cores	**Invited talk**

b. **<u>Organization of Conferences or Sessions</u>**

Date	Name of Conference	Place	Subject of Conference	Role
2018	**ICS**	Beijin, China	**Supercomputer**	**Program chair**
2013	**ISCA conference**	ISRAEL	**International symposium on computer Architecture**	**General Chair**
2010	**ICS**	Greece	**Supercomputer**	**Program committee co-chair**
2008	**ICS**	Japan	**Supercomputer**	**Program committee co-chair**
2007	**PACT**	USA	**Parallel architecture and compilers**	**Tutorial chair**

6 Awards

- 2017- IEEE Fellow
- IAA -- Inter Achievement Award (Highest award in Intel) for leading the CMP architecture for Core Due family
- "2016 Top-10 patent" for Huawei corporation

(I also got tens of "smaller awards"; i.e., best employee of the month, best tutor, etc. from companies I worked for; e.g., Intel, Huawei, National Semi-conductor and in in the academia)

7 Invited Lectures\ Colloquium Talks

(I gave more than 50 invited Lectures/Colloquium talk all around the Globus. Below I mentioned a sample of them)

Date	Place of Lecture	Name of Forum	Presentation/Comments
2017	**Barcelona**	**Distinguish lecture**	**NVDRAM a new technological evolution or a new system revolution?**
2016	**Munich**	**Keynote in "multiprocessors for embedded**	**Hardware and software mechanisms for**

		systems”	**Thermal & Power/Energy management in modern multi-core systems**
2015	**OSLO**	**HiPEAC Conf. keynote speach**	**Heterogeneous systems – a blessing or a curse for massive parallel dependable systems?**
2015	**China (Hangzhou)**	**West-Lake Conference**	**Keynote speech: “Sociotechnology as a drive for innovation**
2014	**UC Irvin - USA**	**Distinguished lecture series**	**The future of heterogeneous massive parallel systems**
2014	**Italy**	**ACACIS (summer school on systems)**	**Course (5 talks) on cloud computing**
2004	**Italy**	**ACACIS (summer school on systems)**	**Course (5 talks) on low power design**

8 Research Grants

a. Grants Awarded

Role in Research	Body granted	Co-Researchers	Topic	Funded by/ Amount	Year
PI	**DoD Israel**		**Reverse Engineeri (Security)**	**350K Shekel for the first year**	**2017 (hopefully will be extended)**
PI	**Ministry of Science, Israel Gov.**	**From the Technion, Prof. Assaf Schuster was co-PI**	**Metro450:**	**~700K$**	**2011-2016**
Subcontractor	**European commissioner (EU)**	**100 companies. The only one from Israel**	EMC^2: support fo the automotive industry	**20KE**	**2015-2017**
PI	**European commissioner (EU)**	**8 institutes around Europe. From Israel the only PI**	EuroLab-4-HPC: Foundations of a European Research Center of Excellence in High Performance Computing Systems	**Horison 2020** **100KE** **(for 2 years, but will be extended)**	**2015-2017**
PI	**European commissioner (EU)**	**EU project. From Israel the only PI**	EU FET (research project) project: Teraflex –future massive parallel systems (>1000 cores).	**EU PF7 350KE**	**2009 - 2012**

PI	**European commissioner (EU)**	**EU Project. In the Technion with Prof. Assaf Schuster**	EU IP project: Encore: Project, build a data-flow based server system	**EU PF7 450KE**	**2009 - 2012**
PI	**European commissioner (EU)**	**EU Project. In the Technion with Prof. Israel Cidon**	EU IP project: Venus-c: Project, build a cloud infrastructure in Europe	**EU PF7 200KE**	**2009-2011**
PI	**Intel**	**Intel Grant**	Computer architecture	**30K$**	**2002 - 2005**

$-US-Dollar, E-Euro, Shelel-Israeli local currency

9 Teaching

a. Courses Taught in Recent Years

These are some of the courses I though

Year	Name of Course	Type of Course	Degree	Number of Students
2017	**Architecture to support machine learning**	**Lecture**	**Graduate level, Technion**	**New course will start next semester**
2016/7	**Hardware Security**	**Lecture**	**Graduate level**	**~15**
2015-2017	**Real-time systems**	**lecture**	**Graduate level, Technion**	**20-30 each time**
2012 - 2017	**Heterogeneous systems**	**Lecture**	**Graduate level, Technion**	**30-55 each time**
2015	**Digital Systems**	**Lecture**	**Undergraduate Technion**	**300**
2013-	**Operating**	**Lecture**	**Undergraduate**	**300 each**

1014	**Systems**		**Technion**	**time**
-2010 2013	**Cloud Computing**	**Lecture/Seminar**	**Graduate level, Technion**	**30**
– 2008 2012	**Low power computers**	**Lecture**	**Graduate level, Technion**	**30**
2000 - 2008	**Computer Architecture**	**Lecture**	**Undergraduate Technion**	**200-300 each time**

10 Supervision of Graduate Students

#	Name of Student	Title of Thesis	Degree	Date of Completion / in Progress	Students' Achievements
1	Leonid Azriel	**Hardware Security**	**Ph.D**	**In Progress**	
2	Chaim Baskin	Streaming processors	**PhD**	**Have just started**	
3	Hamad Yasin	Power and performance monitoring of large systems	**PhD**	**In Progress**	
4	Gil kedar	Schedule for power in real-time based systems	**PhD**	**2017**	**Graduated**
5	Uri Verner	The use of GPGPUs for handling streaming data	**PhD**	**2015**	**Graduated**
6	Efraim Rotem	Power management in Heterogeneous systems	**PHD**	**2015**	**Graduated**
7	Freddy Gabbay	Value prediction techniques for advanced superscalar computers	**PhD**	**1997**	**Graduated**
8	Uri Shomroni	Using machine learning to manage resources of	**MSC**	**In progress**	

		computer systems			
9	Amit Fucks	Fault tolerant OS for 1000's cores on Die system	**MSC**	**In progress**	**Expect to graduate soon**
10	Leor Bar-Lev	Fault tolerant mechanisms on NoC	**MSC**	**In-progress**	**Just started**
11	Shani Rochana	The use of Deep-Learning as part of modern computer architecture	**MSC**	**In-Progress**	**On Maternity leave**
12	Oren Nishri	PUF architecture	**MSC**	**In-Progress**	**About to graduate**
13	Natalie Katz	CANBUS architecture	**MSC**	**In-Peogress**	
14	Orit Faina	Security models	**MSC**	**In-Progress**	
15	Natan Liss	Design methodologies for FPGA	**MSC**	**In-Progress**	
16	Chaim Baskin	Streaming processors	**MSC**	**2017**	**Graduate**
17	Rami Jeissy	Power efficient scheduling in Heterogeneous systems	**MSC**	**2015**	**Graduate**
18	Ahmad Yasin	Enhanced performance and power monitoring techniques	**MSC**	**2015**	**Graduate**
19	Leonid Azriel	The use of peripheral I/O processor	**MSC**	**2014**	**Graduate**

20	Idan Igra	User provided code for conflict resolution in transactional memory	**msc**	**2013**	**Graduate**
21	Gad Yuval	Next generation of DSP architectures	**MSC**	**2013**	**Graduate**
22	Igor Tolchinsky	Tile Affinity	**MSC**	**2013**	**Graduate**
23	Roman Malits	New scheduling algorithm for Graphics processors	**MSC**	**2011**	**Graduate**
24	Anton Lavron	Hybrid Dataflow + control flow execution model	**MSC**	**2011**	**Graduate**
25	Chen Damishian	New cache prefetching mechanism	**MSC**	**2010**	**Graduate**
26	Shmulik Zobel	Power and performance issues in GPU architectures	**MSC**	**2010**	**Graduate**
27	Iris Sorani	Characterization of long-traces and their applications	**MSC**	**2008**	**Graduate**
28	Ron Gabor	Scheduling and fairness in multi core – shared memory systems	**MSC**	**2007**	**Graduate**
29	Ishay Geler	Advance predetching techniques	**MSC**	**2007**	**Graduate**
30	Behar Michael	Filter trace cache	**MSC**	**2006**	**Graduate**

31	Avi Timor	Re-execution – adding support for soft error recovery at the processor level	**MSC**	**2006**	**Graduate**
32	Oren Katzengold	The use of "non executable machine instructions (Pragma) for improving the utilization of the processor resources	**MSC**	**2006**	**Graduate**
33	Alexander Gendler	New hybrid based data prefetching techniques	**MSC**	**2005**	**Graduate**
34	Shomar Bishara	Fragmented line cache – a new cache structure for saving bus bandwidth	**MSC**	**2003**	**Graduate**
35	Assad Khamaisee	Integrating Value prediction and trace cache techniques	**MSC**	**2003**	**Graduate**
36	Oleg Kosyakovsky	Using feedback directed optimizations to reduce power and improve performance of trace-cache systems	**MSC**	**2002**	**Graduate**
37	Menaker Ohad	Survey on multi-threaded systems and applications	**ME**	**1997**	**Graduate**

38	Vinov Michael	The use of inter-instructions parallelism and its use for designing new architectures	**MSC**	**1996**	**Graduate**
39	Bekerman Michael	Design alternatives for multi-streams architectures	**MSC**	**1996**	**Graduate**
40	Shavit Nira	New approach for load balance in Network based computer systems	**MSC**	**1996**	**Graduate**
41	Gabbay Freddy	TOMESI - A new cache coherency protocols for distributed multi-cache systems	**MSC**	**1995**	**Graduate**
42	Ohad Falik	Using buffers as an alternative to caches in parallel architectures	**MSC**	**1995**	**Graduate**
43	Naftaly Ramaty	The use of fault tracking for debugging real-time applications	**MSC**	**1995**	**Graduate**
44	Zimmerman Ofer	Write cache as alternative to write back caches	**MSC**	**1994**	**Graduate**
45	Avi Bitan	Asymptotic performance evaluation of computer memory models”	**MSC**	**1993**	**Graduate**

46	Ayelet Bak	An extension of the analytical cache model"	**MSC**	**1993**	**Graduate**

11 Professional Experience

PROFESSIONAL EXPERIENCE

- 2015 - Current CTO Optitura LTD**.**
- 2016 – Current Consultant to Shannon Labs, Huawei, China
- 2013 – 2015 Consultant to Shannon Labs, Huawei, China
- 2009 - 2012 Microsoft R&D Israel, manager of the Academic outreach and external research, Israel
- 1999 - 2009 Intel, Principle Engineer, architect for future micro-architecture, mobility Group, Israel

  His role included
  - Senior member of the research group
  - Architect of the CMP features in Core Due family – got the IAA (Inter Achievement Award) for this work
  - Work on accelerators and different GPGPU aspects (HW and SW)
  - Part of the small team that worked on the definition of next generation processor architecture (2015)
- 1997 – 1999 National Semiconductors, Head of the PC research Lab, senior chip architect and a senior member of the PC-on-a-chip (GEOD) team
- 1979 – 1990 Rafael- Director of a software engineering group and in charge of research in Object Oriented techniques and formal methods for developing real-time systems

SIGNIFICANT PROFESSIONAL PROJECTS (part of his industrial activities)

- Architect of the CMP feature of Intel Core-Due family of processors. These work considered to be a break-through in the design of modern processors, since was the first one to trade frequency with multiple cores on die, since we understood that power will govern the design of modern architectures**.**

- As part of my work in Intel, I was deeply involved in the process of defining the power management support for the CMP architectures such as in Core-Due family**.**
- Few of the research topics I initiated and lead while in Intel research (MRL) were implemented few years later and are part of the current products or most likely will be part of the next generation cores**.**
- Part of the architecture team of the first “System-on-Chip” National produce. This work considered to be a breakthrough in designing System-On-Chip (SoC) architecture. The design included revolutionary aspects of mixed-signal design, integration methodologies, new testing methodologies, new SW/HW interfaces and more
- Help to design of Next Generation Data-Center for Huawei Shannon Lab

12 PUBLICATIONS

12.1 Refereed papers in professional journals

Published papers

1. Zhibin Yu, Wen Xiong, Lieven Eeckhout, Zhendong Bei, Mendelson Avi, Chengzhong Xu, "MIA: Metric Importance Analysis for Big Data Workload Characterization", IEEE Transactions on Parallel and Distributed Systems, to be published during 2017.
2. Leonid Azriel, Ran Ginosar and Avi Mendelson, "Using Scan Side Channel to Detect IP Theft" – accepted for publication in the IEEE Transactions on VLSI, 2017
3. G. Kedar, A. Mendelson and I. Cidon, "SPACE: Semi-Partitioned CachE for Energy Efficient, Hard Real-Time Systems," in IEEE Transactions on Computers, vol. 66, no. 4, pp. 717-730, April 1 2017.
4. G. Kedar, A. Mendelson and I. Cidon, "Energy Oriented EDF for Real-Time Systems" to be published in IJES, 2017
5. Jawad Haj-Yihia, Ahmad Yasin, Yosi Ben Asher, and Avi Mendelson, "Fine-Grain Power Breakdown of Modern Out-of-Order Cores and Its Implications on Skylake-Based Systems.", in *ACM Trans. Archit. Code Optim.* 13, 4, Article 56 (December 2016)
6. Uri Verner, Avi Mendelson, Assaf Schuster, "Extending Amdahl's Law for Multicores with Turbo Boost", to be presented in IEEE Computer Architecture Letters
7. Rotem Efraim, Uri C. Weiser, Avi Mendelson, Ran Ginosar, Eli Weissmann, Yoni Aizik, Intel Corporation "H-EARtH: Heterogeneous Multi-Core Platform Energy Management" to appear in a special issue of IEEE Computer, on Energy-Efficient Computing, 2016
8. S. Weis, A. Garbade, B. Fechner, A. Mendelson, R. Giorgi and T. Ungerer: "Architectural Support for Fault Tolerance in a Teradevice Dataflow System", International Journal of Parallel Programming (IJPP), Springer, February, V2, PP 218—232, 2016

9. Efraim Rotem, Ran Ginosar, Avi Mendelson, Uri C. Weiser “Power and thermal constraints of modern system-on-a-chip computer” Microelectronics Journal, Elsevier, December, 2015, pp 1225-1229

10. Leonid Azriel , Avi Mendelson, Uri C Weiser, “Peripheral Memory: a Technique for Fighting Memory Bandwidth Bottleneck”, in *IEEE Computer Architecture Letters*, vol. 14, no. 1, pp. 54-57, Jan.-June 1 2015

11. R. Giorgi et al., “TERAFLUX: Harnessing dataflow in next generation teradevices”, Microprocessors and Microsystems 01/2014; http://dx.doi.org/10.1016/j.micpro.2014.04.001

12. Rotem, E. ; Ginosar, R.; Weiser, U.; Mendelson, A. “Energy Aware Race to Halt: A Down to EARtH Approach for Platform Energy Management”. IEEE Computer Architecture Letters – pp 1-4, Oct 2012

13. R Malits , E Bolotin, A Kolodny, A Mendelson, “Exploring the limits of GPGPU scheduling in control flow bound” applications ACM Transactions on Architecture and Code Optimization (TACO) 8 (4), 29

14. Timor , A. Mendelson, Y. Birk and N. Suri, “Using Under-Utilized CPU resources to Enhance its Reliability" IEEE Trans. Dependable Sec. Comput. 7(1): 94-109 (2010)

15. Z. Guz , E. Bolotin, I. Keidar, A. Kolodny, A. Mendelson, and U. Weiser, “Many-Core vs. Many-Thread Machines: Stay Away From the Valley”, in Computer Architecture Letters, January-June 2009 (vol. 8 no. 1), pp. 25-28

16. R. Gabor , S. Weiss and A. Mendelson, “Service Level Agreement for Multithreaded Processors” ACM Transactions on Architecture and Code Optimization, Volume 6 , Issue 2 (June 2009)

17. R. Gabor , S. Weiss and A. Mendelson, " Fairness Enforcement in Switch on Event Multithreading", ACM Transactions on Architecture and Code Optimization (TACO), Volume 4 , Issue 3 (September 2007)

18. M. Behar , A. Mendelson and A. Kolodny, ” Trace Cache Sampling Filter", in ACM Trans. Computer. Systems, V25, N1, PP 28-35, 2007.

19. Alex Gontmakher , Assaf Schuster and Avi Mendelson: Inthreads: a low granularity parallelization model, in ACM SIGARCH Computer Architecture News, v.34 n.1, p.77-80, March 2006

20. Alon Naveh, Efraim Roterm, Avi Mendelson, Simcha Gochman, Rajshree Chabukswar, Karthik Krishnan, Arun Kumar , "Power and Thermal Management in the Intel® Core™ Duo Processor Architecture" in Intel Technology Journal, Volume 10, issue 02, pp 109-122, 2006.

21. Avi Mendelson, Julius Mandelblat, Simcha Gochman, Anat Shemer, Rajshree Chabukswar, Erik Niemeyer, Arun Kumar "CMP Implementation in systems based on the Intel® Core™ Duo Processor Architecture", in Intel Technology Journal, Volume 10, issue 02, pp 99-108 2006.

22. Simcha Gochman, Avi Mendelson, Alon Nave and Efraim Rotem, "Introduction to Intel® Core™ Duo Processor Architecture" in Intel Technology Journal, Volume 10, issue 02, pp 89-98 2006.

23. Alexander Gendler and Avi Mendelson and Yitzhak Birk, "A PAB-Based multi-prefetcher Mechanism", International Journal of Parallel Programming" 34(2): 171-188 (2006).

24. A. Cohen, L. Finkelstein, A. Mendelson, R. Ronen, D. Rudoy. *"On Estimating Optimal Performance of CPU Dynamic Thermal Management."* IEEE computer Architecture Letters, V2, Oct. 2003.

25. Baruch Solomon, Avi Mendelson, Ronny Ronen, Doron Orenstein, Yoav Almog: Micro-operation cache: a power aware frontend for variable instruction length ISA. IEEE Trans. VLSI Syst. 11(5): 801-811 (2003)

26. A. Roth and R. Ronen and A. Mendelson: "Dynamic techniques for load and load-use scheduling" in Proceedings of the IEEE , Volume: 89 Issue: 11 , Nov. 2001, Page(s): 1621 –1637

27. Ronny Ronen, Avi Mendelson, Konrad Lai, Shih-Lien Lu, Fred Pollack, and John P. Shen: "Coming Challenges in Microarchitecture and Architecture" in Proceedings of the IEEE , Volume: 89 Issue: 3 , March 2001 Page(s): 325 -340

28. Avi Mendelson and Freddy Gabbay: "The Effect of Seance Communication on Multiprocessing Systems" in ACM Transaction on Computer Systems, V-19 I-2 May 2001, pp 252-281.
29. N. Suri and A. Mendelson, : "Design of a Parallel Interconnect Based on Communication Pattern Considerations" Journal of Parallel Algorithms and Applications, Vol 16, Sept 2001, pp 243-271
30. A. Mendelson and M. Bekerman : "Design Alternatives of Multithreaded Architecture.", Journal of Parallel systems and programming (IJPP), 27(3) Aug. 1999. Pages 161-193.
31. F. Gabbay and A. Mendelson : "The "Smart" simulation Environment -- A tool-set to Develop New Cache Coherency Protocols", Journal of System Architecture 45 (1999) pp 619-632
32. F. Gabbay and A. Mendelson : "Improving Achievable ILP through Value Prediction and Program Profiling." Microprocessors and Microsystems, vol.22, no.6, November 30. 1998. Pages 315-332
33. F. Gabbay and A. Mendelson : "Using Value Prediction to increase the Power of Speculative Execution Hardware", in ACM Transactions on Computer Systems Vol. 16, No. 3 (Aug. 1998), Pages 234-270
34. M. Bekerman and A. Mendelson :"A performance Analysis of Pentium Processor Systems", IEEE Micro, October 1995, pp 72 -83.
35. A. Mendelson and S. Pinter and R. Shtokhamer,: "Optimization techniques for cache based instruction caches", in Computer Architecture Notes, April 1994. (and in Lecture Notes in Computer Science, No. 786, Springer-Verlag, April 1994, pp. 404--418.)
36. A. Mendelson, D. Thiebaut and D.K. Pradhan : "Modeling live and dead lines in cache memory systems", in IEEE Trans. on Computers, pp. 1-16, Jan. 1993.
37. A. Mendelson, D.K. Pradhan and A.D. Singh: "A single cache copy data coherence (sccdc) scheme for multiprocessor systems", in Computer Architecture Notes, PP 36-49, December 1989.

12.2 Chapters in Books

1. A. Mendelson and N. Suri and O. Zimmerman : “Roll-Forward Recovery: The Bi-Directional Cache Approach" in Fault Tolerant Parallel and Distributed Systems (Book), pp59-70
2. A. Mendelson, D. Thiebaut and D.K. Pradhan : “Modeling live and dead lines in cache memory systems", chapter in the book "Performance Modeling for Computer Architecture" edited by C.M. Krishna. Publisher : IEEE Computer Society Press, Los Alamitos, California 1996
3. A. Mendelson and S. Pinter and R. Shtokhamer,: “Optimization techniques for cache based instruction caches" Lecture Notes in Computer Science, No. 786, Springer-Verlag, April 1994, pp. 404--418.
4. Roni Rosner, Yoav Almog, Micha Moffie, Naftali Schwartz and Avi Mendelson, “PARROT: Power Awareness Through Selective Dynamically Optimized Traces” in Lecture Notes in Computer Science, 2005, Volume 3164, Power - Aware Computer Systems, Pages 395-428
5. The chapter “Address value speculation” in the book “Speculative Execution in High Performance Computer Architectures “, PP 187 – 215, Edited by: David Kaeli and Pen Yew
6. “A Programming Model and Architectural Extensions for Fine-Grain Parallelism”, Alex Gontmakher, avi Mendelson, and Assaf Schuster. A chapter in “Parallel Computing: Models, Algorithms, and Applications”. CRC Press, John Reif and Sanguthevar Rajasekaran Ed's. Computer and Information Science Series, Sartaj Sahni chief-editor.”

12.3 Patents

1) 7,558,946 Breaking a lock situation in a processor without detection of the lock situation using a multi-level approach
2) 7,451,333 Coordinating idle state transitions in multi-core processors
3) 7,141,953 Methods and apparatus for optimal voltage and frequency control of thermally limited systems (also 7,586,281) 60143485 TECHNIQUES TO MANAGE POWER FOR A MOBILE DEVICE
4) 6,854,033 Using linked list for caches with variable length data
5) 6,473,777 Method for accelerating java virtual machine bytecode verification, just-in-time compilation and garbage collection by using a dedicated co-processor
6) 5,996,060 System and method for concurrent processing
7) 119252 Systems and Methods for Concurrent Processing (Israeli Patent)
8) 5,930,830: "System and Method for concatenating discontigous memory pages"
9) 7,958,510 "Device, system and method of managing a resource request
10) 7412569 "System and method to track changes in memory"
11) 7251811 "Controlling compatibility levels of binary translations between instruction set architectures"
12) 7047395 "Reordering serial data in a system with parallel processing flows"
13) 7260684 "Trace cache filtering"
14) 8531471, "SHARED VIRTUAL MEMORY"
15) 8397241 (also 8683487)- Language level support for shared virtual memory, 2013
16) 9003421 Acceleration threads on idle OS-visible thread execution units, 2015
17) 9032103 Transaction re-ordering, 2015
18) 20140129808 - Migrating tasks between asymmetric computing elements of a multi-core processor, 2014
19) WO2017012667A1 -- Coherence protocol for hardware transactional memory in shared memory using non volatile memory with log and no lock, 2016

PCI related patents

20) 7,899,943 "Pci express enhancements and extensions -- Atomic and Test&Set", March, 2011
21) 7,930,566 "PCI express enhancements and extensions -- Performance and power optimizations", Apr. 2011
22) 7,949,794 – "Pci express enhancements and extensions – Cache and ACH", May, 2011
23) 8,073,981 – "Pci express enhancements and extensions -- Snoop and Snoop Filter", December, 2011
24) 8,099,523 - "PCI express enhancements and extensions -- transactions having prefetch parameters", Jan. 2012

25) 8,230,119 – “Pci express enhancements and extensions -- RMW”, June 2012
26) 8,230,120 – “Pci express enhancements and extensions -- Loose Events”, July 2012
27) 8,447,888 - Pci express enhancements and extensions, 2013 – Stride I/O operations
28) 8,473,642 – “Pci express enhancements and extensions -- BAR”, June 2013
29) 8,549,183 – “Pci express enhancements and extensions -- Relaxed Ordering”, Oct. 2013
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