Memory Technologies

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Primary Storage

Computer memory that is accessible for the CPU without the use of computer’s IO channels.

- Primary Storage (today)
  - Registers
  - Cache Memory
  - Main storage (RAM)

Volatile storage:
A computer memory that requires power to maintain the stored information.

Non-volatile storage:
Computer memory that can retain the stored information even when not powered.

Historical Background

The first storage device appeared with the invention of first digital computer (1937).

Some things have changed since…

Drum Memory (1932)

- Invented by Gustav Tauschek in 1932 in Austria.
- Used by the first digital computer (ABC) in 1937.
- Widely used in the 1950’s and into 1960’s.

Description:
- Large metal cylinder.
- Coated with Ferromagnetic recording material.
- Divided to tracks around its surface.
- Each track has its own read/write head.
Drum Memory (1932)

**Working Principles:**
- The drum is constantly rotating.
- The read/write head access data by waiting for the required particle to pass it.
- Comparison to today's hard disc.

**Working Principles (cont.):**
- Writing was done by generating an electro magnetic pulse which changed the polarity of the particle.
- Reading was done by detecting which particles were "polarized".

Drum Memory (1932)

The capacity of a drum of 20 cm long and 10 cm in diameter was about 62KB.

The Williams Tube (1946)

- Developed by Freddie Williams and Tom Kilburn in 1946-1947. In University of Manchester.
- A cathode ray tube (CRT) used to electronically store binary data.
- Typically stored 0.1KB.

CRT Principles

- Electron beam draws a spot on the phosphor covered screen in a directed XY position.
- Each electron that hits the screen, releases number of secondary electrons and creates an electric charge.
- The charge persists for ~0.2 seconds after the beam switched off.
The Williams Tube (1946)

- Became unreliable with time, had to be “tuned” manually.
- The medium for first memory stored program (written by Tom Kilburn).
- Used in:
  - British: Ferranti Mark I
  - American: IAS Machine, UNIVAC 1103, IBM 701, IBM 702
  - Soviet: Strela 1

Delay Line Memory (40s-50s)

- Concept originated with WW II radar research.
- Sound Travels Slower than Electricity.
- Mercury delay line memory was invented by John Adam Presper Eckert Jr. for the EDVAC computer.
- At one end of the tube, a transducer converted the electrical pulses to sound, which propagated through the mercury to the other end. At that point, another transducer converted the sound to electricity and sent it back to the beginning.
- EDSAC operated with 512 35-bit words stored in 32 delay lines, ~2KB
- Avg. access time was ~200 microseconds.
- Later versions used metal wires as storage medium instead of mercury.
- Was in use into the late 60s
Core Memory (1949)

- Invented by An Wang / Jay Forester in the early 50s.
- Patent granted to Wang only in 1955 (by that time the core was already in use).

Core Memory (1949)

- The most popular memory device till the late 70's.
- Replaced by semiconductor based memory.
- First used by the IBM 705 in 1955. (100K, 17 microseconds cycle time).
- Prices per bit: 0.2$ in 1960 to 0.01$ in 1976.

Core Memory (1949)

- Non-Volatile memory.
- Unaffected by EMP and radiation.
- Used in fighter aircraft and spacecraft to the late 80's.

Core Memory (1949)

How it works:
- The memory consists of an array of ferrite cores.
- A core is required for each bit of memory.
- Each core has three wires passing through it, providing the means to select and detect the contents of each bit.

Reading:
- Only one X and Y line is driven with a pulse of current.
- If the memory bit accessed is already in the 0 state, the sense/inhibit will not detect a change.
- If the memory bit accessed was in the 1 state, then the combined pulse of current with flip it into a 0 state, and the sense/inhibit will detect the pulse.
Core Memory (1949)

Writing:
- A read cycle must have preceded the write to set all the bits in the word to 0.
- Only one X and Y line is driven with a pulse of current to access the required location. This pulse is in the opposite direction to the read current.
- All other memory locations will at worst, only have half the required magnetic pulse, and will not be affected.

Writing (cont):
- If the memory location is to contain a 0, the sense/inhibit line is driven with sufficient current to neutralize the effect of the XY lines.
- If the memory location is to contain a 1, the sense/inhibit line is not driven, and the XY lines will flip the memory core into the 1 state.

Bubble Memory (1970)
- Non Volatile
- Invented by Andrew Bobeck.
- 1 cm square memory held 0.5 KB.
- Was in use till mid 80’s. Replaced by faster and cheaper hard disks and flash.

Modern Memory Technologies (from 1960s)

Transistor Revolution (late 60s)

Transistor based Memory Technologies
- Random Access Memory
  - DRAM, SRAM
- Read Only Memory –
  - Mask ROM, PROM, EPROM, EEPROM (Flash memory)
Dynamic Random Access Memory (DRAM)

- Volatile
- Refresh Required
- Multiplexed Access

Usage:
Computer Main Memory

DRAM

Invented in 1966 (and patented in 1968) by Dr. Robert Dennard at the IBM Thomas J. Watson Research Center.

Structure:
Each cell consists from:
- 1 transistor
- 1 capacitor

DRAM cell

First commercially available 1-transistor cell DRAM, the Intel 1103 (1024x1 Bytes) in October 1970

During 1970s no crucial changes in Main Memory technology
Memory modules steadily increasing from 1KB in 1970 to 1MB in the early 80s.
1981 – Bill Gates claims that 640 KB will be enough for any future applications.
Therefore, the new operating system - DOS doesn’t support memories larger than 640KB.
Though, some alternative methods of using extra memory are developed.
**Evolution of DRAM:**

**Asynchronous DRAM:**
- Fast Page Mode (FPM DRAM) 1987
- Extended Data Out (EDO DRAM) 1993
- Burst EDO (BEDO DRAM) 1995

**Synchronous DRAM:**
- Synchronous (SDRAM) 1996
- Rambus (RDRAM) 1999
- Double Data Rate (DDR SDRAM) 2000
- Double Data Rate 2 (DDR2 SDRAM) 2003
- Double Data Rate 3 (DDR3 SDRAM) 2007

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**FPM DRAM (1987)**

*(Fast Page Mode)*

Improvement over basic model:
Fast successive accesses to the same page of memory.

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**EDO DRAM (1993)**

*(Extended Data Out)*

Improvement over FPM:
A new access cycle can be started while keeping the data output of the previous cycle active.
This allows a certain amount of overlap in operation (pipelining), allowing somewhat improved speed.
It was 5% faster than FPM DRAM.

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**BEDO DRAM (1995)**

*(Burst Extended Data Out)*

Improvement over EDO:
Could process 4 memory addresses in one burst.

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**SDRAM (1996)**

*(Synchronous)*

Memory Clock Cycle: 66 – 150 MHz
Bus Clock Cycle: same
Transfer Rate: 1.2 – 6.4 GB/sec

- First fully synchronous with CPU and memory bus
- Overcame the 66MHz limit of the asynchronous models

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**RDRAM (1999)**

*(Rambus)*

Memory Clock Cycle: 300-800MHz
Transfer Rate: 1.2 – 6.4 GB/sec

- Developed by Rambus company
- Supported by Intel for its Pentium processor
- Although very advanced technology, it failed commercially so far for different reasons.
(Double Data Rate)

- Memory Clock Cycle: 100-200MHz
- Bus Clock Cycle: 200-400 MHz
- Transfer Rate: 1.6 - 3.2 GB/sec
- Common module sizes: 128MB-1GB

- Transfers data on the rising and falling edges of the clock signal.
- Effectively, it nearly doubles the transfer rate without increasing the frequency of the front side bus.

**DDR2 SDRAM (2003)**
(Double Data Rate 2)

- Memory Clock Cycle: 100-266MHz
- Bus Clock Cycle: 200-400 MHz
- Transfer Rate: 1.6 - 3.2 GB/sec

**DDR3 SDRAM (2007?)**
(Double Data Rate 3)

- Prototypes were announced in early 2005

memory Clock Cycle: 100-200 MHz
- Bus Clock Cycle: 400-800 MHz
- Peak Transfer Rate: 6.4 - 12.8 GB/sec

**Static Random Access Memory (SRAM)**

- Volatile
- NO refresh Required
- Fully Random Access

*Usage:* Cache Memory

**SRAM (vs. DRAM)**

- More expensive
- Less dense
  **But**
  - Faster
  - Less power consumption
  - Easier to control
  - More truly "random access"
  - No need for constant refresh

**SRAM cell**

- SRAM cell consists of 6 transistors:
  - 4 of them form two cross-coupled inverters for state holding (1 or 0)
  - 2 are access transistors, serve to control the access to the storage cell
Read Only Memory (ROM)

- **Types:**
  - Mask ROM (ROM) before transistors
  - Programmable ROM (PROM) 1956
  - Erasable PROM (EPROM) 1971
  - Electronically Erasable PROM (EEPROM) 1983
  (Flash is a later type of EEPROM – 1984 by Dr Fujio Masuoka)

Mask ROM
- The data is physically encoded in the circuit, so it can only be programmed during fabrication

**Advantages:**
1. Cheap if bought in large quantities
2. Compact

**Disadvantages:**
1. One-Time masking cost is high
2. Long production time
3. Impractical for Research & Development
4. Unrecoverable from errors

Programmable ROM
- PROM was invented in 1966 by Wen Thing Chow
- The key difference from a strict ROM is that the programming is applied after the device is constructed
- Solves first 2 problems of Mask ROM

Erasable Programmable ROM (EPROM)
- EPROM was invented in 1971
- The programming can be modified for design needs
- Solves the 3rd problem of Mask ROM as well

EPROM
- Intel C4702A

EPROM
- EPROM Translator/Cell
  - Silicon Oxide Diaphragm
  - metal tracks
The difference between EPROM and EEPROM lies in the way that the memory programs and erases. EEPROM can be programmed and erased electrically using field emission (more commonly known in the industry as “Fowler-Nordheim tunneling”).

- Solves all 4 problems
- Developed in 1983 by George Perlegos

Flash Memory

- Is a type of EEPROM, developed by Dr. Fujio Masuoka while working for Toshiba in 1984
- Intel saw the massive potential of the invention and introduced the first commercial flash chip in 1985
- Toshiba announced NAND flash at ISSCC in 1989
Flash Memory

- Stores information in an array of floating-gate transistors, called "cells".

RAM vs. ROM vs. Flash

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