Fast Concurrent Queues for x86 Processors

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Abstract
Conventional wisdom in designing concurrent data structures is to use the most powerful synchronization primitive, namely compare-and-swap (CAS), and to avoid contended hot spots. In building concurrent FIFO queues, this reasoning has led researchers to propose combining-based concurrent queues.

This paper takes a different approach, showing how to rely on fetch-and-add (F&A), a less powerful primitive that is available on x86 processors, to construct a nonblocking (lock-free) linearizable concurrent FIFO queue which, despite the F&A being a contended hot spot, outperforms combining-based implementations by 1.5× to 2.5× in all concurrency levels on an x86 server with four multicore processors, in both single-processor and multi-processor executions.

Categories and Subject Descriptors D.1.3 [Programming Techniques]: Concurrent Programming; E.1 [Data Structures]: Lists, stacks, and queues

Keywords concurrent queue, nonblocking algorithm, fetch-and-add

1. Introduction
Avoiding contended hot spots is a fundamental principle in the design of concurrent algorithms [13]. The concurrent FIFO queue, a fundamental and commonly used data structure, is a prime example of this principle in action: Both of Michael and Scott’s classic algorithms [19], one lock-based and one nonblocking, do not scale past a small amount of concurrency because threads contend on the queue’s tail and head [11][13]. To get around this seemingly inherent bottleneck, researchers have recently applied combining approaches in which one thread gathers pending operations of other threads and executes them on their behalf [7][8][11].

Most non-combining concurrent algorithms synchronize using compare-and-swap (CAS) loops: a thread observes the shared state, performs a computation, and uses CAS to update the shared state. If the CAS succeeds, this read-compute-update sequence appears to be atomic; otherwise the thread must retry. Essentially, the idea behind combining is that the synchronization cost of a contended CAS hot spot (due to cache coherency traffic on the contended location) is so large that performing all the work serially, to save synchronization, performs better [11]. In this paper we show that the truth is more nuanced: it is work wasted due to CAS failures that largely causes the poor performance of algorithms with a CAS hot spot, not just the synchronization cost.

Observing this distinction, let alone exploiting it, is not possible on most commercial multicore architectures which only support the universal primitives CAS or load-linked/store-conditional (LL/SC). While in theory these can implement weaker primitives in a wait-free manner [12], such implementations are heavyweight and in practice vendors direct programmers to use CAS loops [1]. However, there is an interesting exception: the (64 bit) x86 architecture, which dominates the server and desktop markets, directly supports various theoretically weaker primitives whose crucial property for our purpose is that they always succeed (see Table 1).

Consider, for example, the fetch-and-add (F&A) primitive. Figure 7 shows the difference in the time it takes a thread to increment a contended counter on a modern x86 system when using F&A vs. a CAS loop. Avoiding the retries and paying only the synchronization price leads to a 4×–6× performance improvement. In this paper we transfer this insight to the domain of FIFO queues, henceforth simply queues.

Our contribution We present LCRQ, a linearizable nonblocking FIFO queue that uses contended F&A objects to spread threads among items in the queue, allowing them to enqueue and dequeue quickly and in parallel, in contrast the inherently serial behavior of combining-based approaches. As a result, LCRQ outperforms prior queue implementations by 1.5× to 2.5× on a system with four Intel Xeon E7-4870 multicore processors, both on single-processor and on multi-processor executions. Because LCRQ is nonblocking, it maintains its performance in oversubscribed scenarios in which there are more threads than available hardware threads. In such workloads it outperforms by more than 20× lock-based combining queues, which cannot make progress if a combiner gets scheduled out.

Our LCRQ algorithm is essentially a Michael and Scott linked list queue [19] in which a node is a concurrent ring (cyclic array) queue, CRQ for short. A CRQ that fills up becomes closed to further enqueues, who instead append a new CRQ to the list and begin working in it. Most of the activity in the LCRQ occurs in the individual CRQs, making contention on the list’s head and tail a non-issue. Within a CRQ, the head and tail are F&A objects which are used to spread threads around the slots of the ring, where they synchronize using (uncontended in the common case) CAS.

Table 1: Synchronization primitives supported as machine instructions on dominant multicore architectures.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>compare-and-swap</th>
<th>swap</th>
<th>test-and-set</th>
<th>fetch-and-add</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM</td>
<td>deprecated</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>POWER</td>
<td>LL/SC</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>SPARC</td>
<td>yes</td>
<td>deprecated</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>x86</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>

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One of the CRQ’s distinctive properties compared to prior concurrent circular array queues \cite{2,4,9,10,22,23} is that in the common case an operation accesses only the CRQ’s head or tail but not both. This reduces the CRQ’s synchronization cost by a factor of two, since the contended head and tail are the algorithm’s bottleneck.

2. Related work

We refer the reader to Michael and Scott’s extensive survey \cite{19} for discussion of additional work that predates theirs.

List based queues Michael and Scott present two linked list queues, one nonblocking (henceforth MS queue) and one lock-based. However, due to contention on the queue’s head and tail, their algorithms do not scale past a low level of concurrency \cite{7,11}. Kogan and Petrank introduce a wait-free variant of the MS queue with similar performance characteristics \cite{16}. Several works attempt to improve the MS queue’s scalability, however all these still suffer from the CAS retry problem \cite{15,17,20}.

Cyclic array queues Prior concurrent cyclic array queues are bounded and can contain a fixed number of items. One of the challenges in these algorithms is correctly determining when the queue is full and empty. The queues of Gottlieb et al. \cite{10} and of Freudenthal and Gottlieb \cite{9} maintain a size counter that is updated using F&A. Such a F&A might bring the queue into an inconsistent state (e.g., size < 0) and the algorithm then tries to recover using a compensating F&A. Still, the inconsistent states make these queues non-linearizable \cite{1}. Blelloch et al. \cite{3} use room synchronization, which prevents enqueues from running concurrently to de-queues, to construct a queue that is linearizable despite temporarily entering inconsistent states when its head/tail are updated using F&A. Another queue by Blelloch et al. \cite{3} avoids inconsistent states of the head and tail by updating these indices using hardware memory block transactions which are not supported by commercial hardware. Tsigas and Zhang \cite{23}, Colvin and Groves \cite{4} and Shafiei \cite{22} present cyclic array queues that avoid inconsistent head and tail states by performing the updates using CAS, but are therefore prone to the CAS failure effect.

In contrast to these prior designs, LCRQ is an unbounded queue formed by linking CRQs (array queues) in a list, with a new CRQ added when an enqueue operation fails to make progress. The ability to close a CRQ, forcing enqueues to move to the next CRQ in the list, makes LCRQ nonblocking whereas prior F&A-based designs \cite{2,3,9,10} are blocking. In addition, since we do not need to determine when the queue is full in a linearizable way, we can recover from inconsistent states that result from using F&A for head/tail updates without compromising linearizability. Performance-wise, a CRQ operation accesses only one end of the queue in the common case, whereas the operations in the previous designs access both the head and tail indices.

Combining Researchers have recently shown that combining-based queues scale better than CAS-based list queues \cite{7,8,11}. A combining algorithm is essentially a universal construction \cite{12} that can implement any shared object. The idea is that a single thread scans a list of pending operations and applies them to the object. Such algorithms greatly reduce the synchronization cost of accessing the object, at the cost of executing work serially.

Hendler et al. describe a linked list queue based on flat combining, a lock-based combining construction \cite{11}. Fatourou and Kallimanis present SimQueue \cite{8}, a queue based on a wait-free combining construction, and CC-Queue, a queue based on a blocking combining algorithm \cite{7}. Section 5 details these algorithms.

Both of Fatourou and Kallimanis’ algorithms use weak synchronization primitives (F&A and SW AP). However, they do so to reduce the synchronization cost of the combining algorithm, which still needs to perform serial work that is linear in the number of threads. In contrast, we use F&A to enable parallelism in the seemingly inherently sequential FIFO queue.

3. Preliminaries

System model Most concurrent algorithms work assumes a sequentially consistent shared memory system, particularly for correctness proofs, as this allows modeling the execution as a sequence of interleaved memory operations performed by the threads. While the x86 memory model is not sequentially consistent, the only difference is that on the x86 a write gets buffered in a write buffer before reaching the memory, allowing a read to be satisfied from memory before a write preceding it becomes globally visible \cite{21}.

However, in our algorithms threads write to shared data only with atomic operations, such as CAS and F&A. Atomic operations flush the write buffer and are globally ordered \cite{21}, allowing us to treat the system as sequentially consistent. Formally, we have a set
of \(T\) sequential threads that communicate by performing operations on the shared memory, as described below.

**Memory operations** The memory is an array of locations, each holding a 64-bit value. We use the notation \(m[a]\) for the value stored in address \(a\) of the memory. Our algorithms use the following primitives supported by the x86 architecture: (1) read(a) which returns \(m[a]\), (2) fetch-and-add, denoted F&A(a,x), which returns \(v = m[a]\) and changes \(m[a]\)'s value to \(v+x\), (3) swap, denoted SWAP(a,x), which returns \(v = m[a]\) and changes \(m[a]\)'s value to \(x\), (4) test-and-set, denoted T&S(a), which returns \(v = m[a]\) and changes \(m[a]\)'s value to 1, (5) compare-and-swap, denoted CAS(a,o,n), which changes \(m[a]\)'s value to \(n\) if \(m[a] = o\) and returns TRUE, or returns FALSE otherwise, (6) compare-and-swap2, denoted CAS2(a,(o0,o1), (n0,n1)), which changes \(m[a]\)'s value to \(n0\) and \(m[a]+1\)'s value to \(n1\) if \(m[a] = o0\) and \(m[a]+1 = o1\) before returning TRUE, or else returns FALSE.

**Concurrent objects** The threads implement a high-level object defined by a specific implementation, a state machine specifying the object’s states and the operations used to transition between the states. Here we are concerned with the FIFO queue, an object whose state, \(Q\), is a (possibly empty) sequence of items. It supports an enqueue\((x)\) operation that appends \(x\) to \(Q\) and returns OK, and a dequeue\(()\) operation which removes the first item \(x\) from \(Q\) and returns \(x\), or returns EMPTY if \(Q\) is the empty sequence.

**Implementations, executions and linearizability** We use the standard definitions of a high-level object implementation and its execution [13]. Our correctness condition is linearizability [13], which (informally) requires that a high-level operation appears to take place at one point in time during its execution interval.

**Progress** According to Herlihy’s now standard definition [12], an implementation is nonblocking if it guarantees that some thread completes an operation in a finite number of steps. In other words, an individual operation may starve, but some operation always makes progress. This guarantee still allows some undesirable scenarios for queues, e.g., an execution in which enqueuers are starved by dequeuers returning EMPTY. Nonblocking queues in the literature [4][19][22][23] actually provide a stronger guarantee, which we call op-wise nonblocking: some enqueue\(()\) completes in a finite number of steps by enqueuing threads, and some dequeue\(()\) completes in a finite number of steps by dequeuing threads.

4. The LCRQ algorithm

LCRQ can be viewed as a practical realization of the following simple but unrealistic queue algorithm (Figure 2). The algorithm represents the queue using an infinite array, \(Q\), with (unbounded) head and tail indices that identify the part of \(Q\) which may contain items. Initially, each cell \(Q[i]\) is empty and contains a reserved value \(\bot\) that may not be enqueued.

An enqueue\((x)\) operation obtains a cell index \(i\) via a F&A on tail. The enqueue then atomically swaps the value in \(Q[i]\) with \(x\). If the swap returns \(\bot\), the enqueue operation completes; otherwise, it repeats this process.

A dequeue, \(D\), obtains a cell index \(h\) using F&A on head and atomically swaps the value in \(Q[h]\) with another reserved value \(\top\). If \(Q[h]\) contained some \(x \neq \bot\), \(D\) returns \(x\). If \(D\) finds \(\bot\) in \(Q[h]\), the fact that \(D\) stored \(\top\) in the cell guarantees that an enqueue operation which later stores an item in \(Q[h]\) will not complete. \(D\) then returns EMPTY if \(\text{tail} \leq h+1\) (\(h+1\) is the value of head following \(D\)'s F&A). If \(D\) cannot return EMPTY, it repeats this process.

While this algorithm is a linearizable FIFO queue 4 it has two major flaws that prevent it from being relevant in practice: using an infinite array and susceptibility to livelock (a dequeuer continuously swaps \(\top\) into the cell an enqueuer is about to access). We obtain the practical LCRQ algorithm by solving these problems.

Our array queue, CRQ, transforms the infinite array to a cyclic array (ring) of \(R\) nodes. The head and tail indices still strictly increase, but now the value of an index modulo \(R\) specifies the ring node it points to. Since now more than one enqueuer and dequeuer can concurrently access a node, we replace the infinite array queue’s SWAP-based exchange with a CAS2-based protocol. This protocol is unique in that, unlike prior work [2][10], an operation does not have to wait for the completion of operations whose F&A returns smaller indices that also point to the same ring node.

The CRQ’s crucial performance property is that in the common fast path, an operation accesses only one F&A. We use the additional synchronization in the ring nodes to detect corner cases, such as an empty queue. Since head and tail are heavily contended, our approach halves an operation’s synchronization cost in the common case. We detail the CRQ algorithm in Section 4.1.

The LCRQ algorithm (Section 4.2) builds on CRQ to prevent the livelock problem. We represent the queue as a linked list of CRQs. An enqueue\((x)\) operation failing to make progress in the tail CRQ closes it to further enqueues. Upon noticing the tail CRQ is closed, each enqueuer tries to append a new CRQ, initialized to contain its item, to the list. One enqueuer succeeds and completes; the rest move into the new tail CRQ, leaving the old tail CRQ with only dequeuers inside it, which allows the dequeuers to complete. The LCRQ is thus op-wise nonblocking.

4.1 The CRQ algorithm

The pseudocode of the basic CRQ algorithm appears in Figure 3. The CRQ represents the queue as a ring (cyclic array) of \(R\) nodes, with 64-bit head and tail indices (Figure 3a). An index with value \(i\) points to node \(i\) mod \(R\), which we denote by node\((i)\). We reserve the most significant bit of tail to denote the CRQ’s CLOSED state. We thus make the realistic assumption that both head and tail do not exceed \(R\).

The synchronization protocol in a CRQ ring node needs to handle more cases than the infinite array queue, which only needs to distinguish whether an enqueue or dequeue arrives first at the node. We proceed to describe this protocol and how it handles these cases.

**Node structure** (Figure 3a) Physically, a ring node contains two 64-bit words. Logically, a ring node is a 3-tuple \((i,v)\) consisting of (1) a safe bit \(s\) (used by a dequeuer to notify the matching enqueuer that storing an item in the node is unsafe as the dequeuer will not be around to dequeue it; we explain the details below), (2) an index \(i\), and (3) a value \(v\). Initially, node \(u\)'s state is \((i,u,\bot)\) for every \(0 \leq u < R\).

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2On the x86 these atomic primitives are known as LOCK ADD, XCHG, LOCK BTS, LOCK CMPXCHG and LOCK CMPXCHG16B.

3We are not aware of this property being explicitly pointed out before.
A node can be in one of two states: if its value is ⊥ the node is empty; otherwise the node is occupied. A CRQ operation attempts to transition a node from empty to occupied or vice versa using CAS2. We say that an operation, op, accesses node u using index i if op’s F&A returns i and u = i mod R, and refer to the operation as enq_i or deq_i as appropriate. An operation accessing a node uses the value of the node’s safe bit and index, as described next, to determine whether it can attempt a transition or should obtain a new index and try accessing another node.

**Dequeueing an item** When a node is in an occupied state, (s,i,x), it holds the item x that has been stored by enq_i(x). In this case, only deq_i, the dequeue operation accessing the node using index i – exactly i and not just equal to i modulo R – can return x. Such a dequeue attempts to remove x by performing the transition (s,i,x) → (s,i←R,⊥) using CAS2 (Figure 3b). We refer to this as a dequeue transition.

**Dequeue arrives before enqueue while node is empty** This case occurs when an empty node whose state is (s,i,⊥) is accessed by deq_i with j = i + kR, i.e., before the matching enqueue enq_i completes. Similarly to the infinite array queue, deq_i prevents enq_j from storing its item in the node by performing an empty transition (s,i,⊥) → (s,j + R,⊥) (Line 43). In fact, the empty transition prevents any operation using some index j – kR from performing a transition on the node. This stronger property was not needed in the infinite array queue, where only one enqueuer and one dequeuer ever access a node.

**Enqueueing an item** When a node is in an empty state (s,i,⊥), any enq_j(x) operation with j = i + kR may attempt an enqueue call to the CRQ.

---

Figure 3: Pseudocode of CRQ algorithm.

```c
struct Node {
  safe : 1 bit (boolean)
  idx : 63 bits (int)
  val : 64 bits (int or pointer)
} // padded to cache line size

struct CRQ { // fields are on distinct cache lines
  head : 64 bit int
  tail : struct { closed : 1 bit, t : 63 bits }
  next : pointer to CRQ, initially null
  ring : array of R Nodes, initially node u = <i,u,⊥>
} // padded to cache line size

// local variables
val, idx : 64 bit int
h, t : 64 bit int
node : pointer to Node
closed : boolean
safe : boolean

while (true) {
  h := F&A(&crq.head, 1) // F&A on all 64 bits of tail
  node := &crq.array[t mod R]
  while (true) {
    val := node.val
    if (node.val = ⊥) {
      if (idx = h) { // try dequeue transition
        if (CAS2(node, <safe, h, val>, <safe, h+R, ⊥>)) goto Line 52
      } else { // mark node unsafe to prevent future enqueue
        if (CAS2(node, <safe, idx, val>, <0, idx, val>)) goto Line 52
      }
    }
  }
  goto Line 52
}
// end of while loop, go back to Line 33
// failed to dequeue, check for empty
if (<closed, t>) := crq.tail
if (i ≤ h+1) {
  fixState (crq)
  return EMPTY
}
}

while (true) {
  h := F&A(&crq.tail, 1) // F&A on all 64 bits of tail
  node := &crq.array[1 mod R]
  val := node.val
  if (node.val = ⊥) {
    if ((idx < t) and (node.val = ⊥)) {
      if (CAS2(node, <safe, idx, ⊥>, <0, t, ⊥>)) {
        return OK
      }
    }
  } else { // idxxh and val = ⊥: try empty transition
    if (CAS2(node, <safe, idx, ⊥>, <0, h+R, ⊥>)) goto Line 52
  }
  goto Line 52
}
// failed to enqueue, check for empty
if (<closed, t>) := crq.tail
if (i ≤ h+1) {
  fixState (crq)
  return EMPTY
}
}

fixState (crq) {
  // local variables
  val, idx : 64 bit int
  h, t : 64 bit int
  while (true) {
    t = F&A(&crq.tail, 0)
    h = F&A(&crq.head, 0)
    if (crq.tail ≠ t) continue // continue loop at Line 62
    if (h ≤ t) return // nothing to do
    if (CAS(&crq.tail, t, h)) return
  }
  h := F&A(&crq.tail, t)
  if (h ≤ t) return
  if (CAS(&crq.head, 0, h)) return
  next := &crq.head
  safe := 1 bit (boolean)
  closed := boolean
  // try dequeue transition
  if (CAS2(node, <safe, h, val>, <safe, h+R, ⊥>)) goto Line 52
}
// F&A on all 64 bits of tail
node := &crq.array[1 mod R]
val := node.val
if (node.val = ⊥) {
  if ((idx < t) and (node.val = ⊥)) {
    if (CAS2(node, <safe, idx, ⊥>, <0, t, arg>)) {
      return OK
    }
  } else { // idxxh and val = ⊥: try empty transition
    if (CAS2(node, <safe, idx, ⊥>, <0, h+R, ⊥>)) goto Line 52
  }
  goto Line 52
}
// failed to enqueue, check for empty
if (<closed, t>) := crq.tail
if (i ≤ h+1) {
  fixState (crq)
  return EMPTY
}
```
transition to store \( x \) in the node. If \( s = 1 \), \( \text{enq}_j \) simply performs the transition \( (1,i,\perp) \to (1,j,x) \). However, if \( s = 0 \), \( \text{enq}_j \) needs to make sure that \( \text{deq}_j \) is not the dequeueer that set \( S = 0 \), since then \( \text{deq}_j \) will not dequeue from the node. \( \text{enq}_j \) determines this by checking if \( \text{head} \leq j \) (Line 52), which means that \( \text{deq}_j \) has not yet started. If so, then \( \text{enq}_j \) makes the transition \( (0,i,\perp) \to (1,j,x) \) (Line 53) which undoes the previous unsafe transition. If \( \text{deq}_j \) then starts after \( \text{enq}_j \)’s check that \( \text{head} \leq j \) performs a transition on the node before \( \text{enq}_j \)’s transition, then \( \text{deq}_j \) performs an empty transition (Line 49) which changes the node’s index and causes \( \text{enq}_j \)’s CAS2 to fail.

We now turn to a walk-through of the algorithm’s pseudocode. For simplicity, we describe optimizations in Section 4.1.1 omitting them from the pseudocode.

**Enqueue (Figure 3d)** An enqueue \( \text{enq} \) repeats the following. It obtains an index to a ring node with a F&A on \( \text{tail} \) (Lines 54-55). If the CRQ is closed, \( \text{enq} \) returns CLOSED (Lines 55-56). Otherwise, \( \text{enq} \) attempts an enqueue transition (Lines 57-61). If this fails (because the node is occupied or the CAS2 fails), \( \text{enq} \) decides to give up and closes the queue in one of two cases: (1) \( \text{enq} \)’s index has passed \( \text{head} \) by \( R \) places, indicating a possibly full queue, or (2) \( \text{enq} \) is failing to make progress for a long time (checked by \( \text{starving()} \)) (Lines 77-101).

**Dequeue (Figure 3b)** A dequeue \( \text{deq} \) repeats the following. It obtains an index, \( i \), to a ring node using F&A on \( \text{head} \) (Lines 34-35). It then enters a loop in which it attempts to read a consistent state of the node and perform a transition. If \( h < i \), where \( i \) is the node’s index, then \( \text{deq} \) has been overtaken between its F&A and reading the node, and so it exits the loop (Line 39). If the node is occupied, \( \text{deq} \) attempts a dequeue transition (Lines 40-42). If the node is empty, \( \text{deq} \) attempts an empty transition (Line 39) and exits the loop if successful. Throughout this process, if \( \text{deq} \)’s CAS2 fails (implying the node’s state changes) then \( \text{deq} \) restarts the loop of reading the node and performing a transition. Whenever \( \text{deq} \) exits the loop without successfully dequeuing an item, it verifies that the queue is not empty before trying to dequeue with a new index (Line 53-54). If the queue is empty, \( \text{deq} \) fixes (see below) the queue’s state so that \( \text{head} \leq \text{tail} \) before returning EMPTY (Lines 55-56).

**Fixing the queue state (Figure 3c)** A dequeueor F&A may bring the queue into an invalid state in which \( \text{head} > \text{tail} \). In such a case, the dequeueor can just perform an empty transition and return EMPTY. However, doing so prevents the enqueueor with the same index from using the node, forcing it to F&A a new node and increasing contention. To avoid this problem, a dequeueor always verifies that \( \text{head} \leq \text{tail} \) before returning EMPTY (Lines 62-74).

### 4.1 Optimizations

#### Bounded waiting for matching enqueues

When an enqueue and dequeue operation using the same index are active concurrently, the dequeueer may arrive at the node before the matching enqueueer. Performing an empty transition in such a case just leads to both operations restarting and accessing the F&A again, needlessly increasing contention on \( \text{head} \) and \( \text{tail} \).

To avoid this, before performing an empty transition (Line 45), a dequeue operation checks whether \( \text{tail} \geq h + 1 \), where \( h \) is the dequeueor’s index. If so, then the matching enqueueer is active and the dequeueer spins for a short while, waiting for the enqueueer transition to take place. Only after timing out on this spin loop does the dequeueer perform an empty transition.

#### Hierarchy awareness

Large servers are typically built hierarchically, with clusters of cores such that inter-core communication inside a cluster is cheap, but cross-cluster communication is expensive. For example, in a multiprocessor system a cluster consists of all the cores on a (multicore) processor. In these hierarchical machines, creating batches of operations that complete on the same cluster without interference from remote clusters reduces synchronization cost.

To achieve this, we add a cluster field to the CRQ, which identifies the current cluster from which most operations should complete. Before starting a CRQ operation, a thread checks if it is running on a cluster. If not, the thread waits for a while, and then CASes cluster to be its cluster and enters the algorithm (even if the CAS fails). Similarly to prior NUMA-aware lock-based algorithms [5, 7], this divides the execution into segments such that in each segment most operations in the CRQ are from the same cluster. However, our optimization does not rely on locks nor does it introduce blocking, as every operation eventually enters the CRQ.

### 4.1.2 CRQ linearizability proof

The CRQ is not a standard FIFO queue because an enqueue can return CLOSED. To deal with this we give the CRQ the semantics of a tantrum queue: a queue in which an enqueue can nondeterministically refuse to enqueue its item, returning CLOSED instead and moving the queue to a CLOSED state. When a tantrum queue is in the CLOSED state, every enqueue operation returns CLOSED without enqueuing its item.

In the following, we prove that CRQ is a linearizable tantrum queue. Let \( E = e_1, e_2, \ldots \) be a possibly infinite execution of CRQ. We assume every thread whose next local step is to complete does indeed complete in \( E \). We denote an operation \( op \in \{\text{enq}, \text{deq}\} \) that returns \( \text{ret} \) in \( E \) by \( \langle op : \text{ret} \rangle \). We now describe a procedure \( P \) (Figure 4) to assign linearizations points to the operations in \( E \).

Essentially, the linearization order of \( \langle \text{enq}(x) : \text{OK} \rangle \) operations is by the index the enqueueer uses when successfully enqueuing its item, and similarly \( \langle \text{deq}(x) : \text{x} \rangle \) operations (\( x \neq \text{EMPTY} \)) are linearized in the order of the index used to dequeue. The trick is to order enqueues and dequeues consistently, since for example a dequeueer’s F&A returning index \( i \) can occur before the corresponding enqueueer’s F&A.

To do this, we track the CRQ’s state at each point in \( E \) using an auxiliary sequential queue. The auxiliary queue consists of an
infinite array, \( Q \), coupled with indices \( \text{head}(Q) \) and \( \text{tail}(Q) \) representing \( Q \)'s head and tail. (Note that \( Q \) is not cyclic.) Initially, \( \text{tail}(Q) = \text{head}(Q) = 0 \) and \( Q[i] = \perp \) for all \( i \).

We process the execution one event at a time, in order of execution, but using information about future events to decide when to linearize an operation. When we linearize an operation we also apply it to the auxiliary queue. We linearize an \( \text{enq}(x) : \text{OK} \) on its final F&A, the one returning index \( i \) such that the operation enqueues \( x \) in \( \text{node}(i) \). At this point we also set \( \text{tail}(Q) \) to \( i + 1 \). We linearize the dequeue of item \( x = Q[h] \) as soon as the dequeue becomes active and \( h \) is the lowest indexed non-\( \perp \) cell in \( Q \), and set \( \text{head}(Q) \) to \( h + 1 \) at this point. We linearize a \( \text{deq} : \text{EMPTY} \) on its read of \( \text{tail} \) that returns a value \( \geq \text{head} \) (we later show that \( \text{head}(Q) = \text{tail}(Q) \) at this point). The full pseudocode of \( P \) in Figure 3 also includes the straightforward cases of linearizing \( \text{enq}(x) : \text{CLOSED} \) operations.

By construction, the linearization point of an operation is within its execution interval, and all completed enqueues and all dequeues that return \( \text{EMPTY} \) are linearized. We now show that completed dequeues which do not return \( \text{EMPTY} \) are also linearized. Here we denote by \( \text{enq}(x) \) (the \( \text{enq}(x) : \text{OK} \) operation whose last F&A on \( \text{tail} \) in \( E \) returns \( i \), causing \( P \) to set \( Q[i] := x \) and linearize it. Similarly, we denote a dequeue operation whose last F&A on \( \text{head} \) in \( E \) returns \( i \) by \( \text{deq} \).

**Lemma 1.** Suppose \( P \) linearizes \( \text{enq}(x) \). If there exists a dequeue operation \( \text{deq} \) that performs a F&A on \( \text{head} \) in \( E \) which returns \( i \), then: (1) \( \text{deq} = \text{deq}_i \) (i.e., \( \text{deq} \) performs no further F&As in \( E \)), (2) \( \text{deq} \) returns \( x \) if it completes, and (3) \( P \) linearizes \( \text{deq}(x) \).

Proof. Let \((s, j, k, \perp) \mapsto (i, i, x) \) \( \text{be enq}(x) \)'s enqueue transition storing \( x \) into \( u = \text{node}(i) \) (Figure 3). Notice that \( j \leq i \). If \( \text{deq} \) takes sufficiently many steps after obtaining \( i \) from its F&A on \( \text{head} \), it performs a transition on \( u \) using index \( i \). To see this, notice that \( \text{deq} \) moves on from \( u \) without performing a transition only if it reads an index \( i > j \) from \( u \) (Figure 3a, Line 53). Because \( \text{enq} \)'s transition succeeds, \( \text{deq} \) is the only operation that can move \( u \)'s index beyond \( i \), so this is impossible.

Now, consider \( \text{deq} \)'s transition. It cannot be \((s, k, \perp) \mapsto (i, i + R, \perp) \) (Line 54) since that implies \( \text{enq} \)'s transition fails, \( \text{deq} \)'s transition also cannot be of the form \((s, k, v) \mapsto (0, k, v) \) (Line 54) because then, \( \text{enq} \)'s transition succeeding implies that some enqueue (possibly \( \text{enq} \)) subsequently obtains index \( t \leq i \) and then observes \( \text{head} \leq t \), which is impossible since \( \text{head} > i \). Thus, \( \text{deq} \)'s transition can only be a dequeue of \( x \). Hence (1) and (2) hold.

We prove (3) using induction on \( k \), the number of linearized enqueue operations. For \( k = 0 \) the claim is vacuously true. Suppose now that the \( k \)-th enqueue operation linearized is \( \text{enq}(x) \). If \( \text{deq} \) exists in \( E \), then it does not complete before \( \text{enq}(x) \)'s final F&A which returns \( i \), since otherwise \( \text{deq} \) does not return \( x \), contradicting (2). Therefore, there exists a first event \( e \) in which \( Q[i] = x \) and \( \text{deq}_i \) is active. Thus at some event \( e' \), or at after \( e \), \( Q[i] = x \) and \( \text{deq}_i \) has performed the F&A on \( \text{head} \) which returns \( i \). Let \( \text{idx} = \{ j : j < i, Q[j] \neq \perp \} \) \( \text{at } e' \). For all \( j \in \text{idx} \), \( \text{deq}_i \) starts by \( e' \) (because \( \text{deq}_i \)'s F&A has returned \( i \)) and does not complete before \( e' \) (as that implies it is not linearized before completing, contradicting the induction hypothesis). Therefore, at \( e' \) \( P \) linearizes \( \text{deq}_i \) for all \( j \in \text{idx} \) and subsequently linearizes \( \text{deq}_i \).

To complete the linearizability proof, we must show that our linearization order meets the tantrum queue specification. Because we enqueue to \( Q \)'s tail, dequeue from \( Q \)'s head, and following the first enqueue to return \( \text{CLOSED} \) all enqueues do so, this amounts to showing that the auxiliary queue is empty when we linearize a \( \text{deq} : \text{EMPTY} \) operation. Lemma 2 below implies this, because we linearize a \( \text{deq} : \text{EMPTY} \) when it reads a value \( t \) from \( \text{tail} \).

---

```c
// shared variables on distinct cache lines:
head : pointer to CRQ
tail : pointer to CRQ
crq : pointer to CRQ
crq := a new CRQ initialized to contain
v := dequeue(crq)
if (v ≠ EMPTY) return v
if (crq.next ≠ null) return EMPTY
crq := dequeue(crq)
if (v ≠ EMPTY) return v
CAS(&head, crq, crq.next)
}
}
}
}
}
}
}
)

// local variables
crq, newcrq : pointer to CRQ
crq := newcrq
if (CAS(&crq.next, null, newcrq)) {    // next iteration at Line 155
    continue
}
if (enqueuer(crq, x) ≠ CLOSED)
return OK
newcrq := a new CRQ initialized to contain x
CAS(&crq.next, null, newcrq)
return OK
}
}
}
}
}
}
}
)

// enforce that head ≤ tail
if (head < tail)
return false
```

---

Figure 5: Pseudocode of the LCRQ algorithm, using a linearizable CRQ black box.

(Figure 3a, Line 53) such that \( t ≤ h + 1 \). Where \( h < \text{head} \) is the value that the \( \text{deq} \)'s prior F&A returns (Line 54).

**Lemma 2.** If at event \( e \), \( \text{head} \geq \text{tail} \), then \( \text{head}(Q) = \text{tail}(Q) \).

Proof. Suppose towards a contradiction that \( \text{head}(Q) < \text{tail}(Q) \) at \( e \). Then there exists a minimal \( i \) such that \( Q[i] ≠ \perp \) at \( e \). Because we update \( \text{tail}(Q) \) following the order of F&As on \( \text{tail} \), \( i < \text{tail}(Q) \leq \text{tail} ≤ \text{head} \) at \( e \). Thus, \( \text{deq} \) is active before \( e \) and should have been linearized by \( P \), a contradiction.

In conclusion, we have shown the following.

**Theorem 1.** CRQ is a linearizable implementation of a tantrum queue.

---

4.2 The LCRQ algorithm

We now present LCRQ using the CRQ as a black box. The LCRQ is simply a linked list of CRQs in which dequeuing threads access the head CRQ and enqueuing threads access the tail CRQ (Figure 5a). An enqueue(x) operation that receives a CLOSED response from the tail CRQ creates a new CRQ, initialized to contain \( x \), and links it after the current tail, thereby making it the new tail (Figure 5b). If the head CRQ becomes EMPTY and there is a node linked after it, dequeues move to the next node, after installing it as the new head (Figure 5b).
**Memory reclamation**  A dequeue that successfully changes the head pointer cannot reclaim the memory used by the old CRQ because there may be concurrent operations about to access it (i.e., stalled just before Line 14 or Line 160). We address this problem by using hazard pointers [13] to protect an operation’s reference to the CRQ it is about to access. We omit the details, which are standard.

**Linearizability**  Assuming that the CRQ is a linearizable tantrum queue, proving that LCRQ is a linearizable queue implementation is straightforward:

**Theorem 2.** If CRQ is a linearizable tantrum queue implementation, then LCRQ is a linearizable queue implementation.

Proof. (Sketch) We linearize an enqueue that completes after appending a new CRQ to the list at the CAS which links the new CRQ (Figure 5c, Line 163). We linearize any other completed operation at the point in which its final CRQ operation takes place. The next pointer of a CRQ $q$ changes from null only after $q$ becomes CLOSED, and conversely, after a CRQ $q$ becomes CLOSED no new enqueue completes until a new CRQ is linked after $q$. Thus, if $q_0$ precedes $q_1$ in the list, any $q_1$ enqueue is linearized after any $q_0$ enqueue. Similarly, any $q_0$ dequeue is linearized before any $q_1$ dequeue. Linearizability follows.

**4.2.1 LCRQ nonblocking proof**

In this section, we sketch the proof of the following theorem:

**Theorem 3.** LCRQ is op-wise nonblocking.

An enqueuer that does not complete within a finite number of steps in the tail CRQ closes it. Once the CRQ is closed, every enqueuer taking enough steps tries to append a new CRQ to the LCRQ. The first one to CAS the CRQ’s next pointer (Figure 5c, Line 163) succeeds and completes. Thus, an enqueue operation completes within a finite number of steps by enqueuing threads.

Now, consider a dequeue $deq$ taking an infinite number of steps without completing. Suppose first that $deq$ remains in one LCRQ node, $q$. If enqueuers take infinitely many steps in $q$, then $q$ does not close and so, because $q$’s size is finite, dequeuers remove items from $q$. If enqueuers take only finitely many steps in $q$, then from some point only dequeuers take steps in $q$ and so eventually $q$’s head exceeds its tail. Then $deq$ finds that $q$ is empty (Lines 23–24), enters fixState() but never leaves. Thus, new dequeuers continue to enter $q$ and increment head. Since the number of dequeuers is finite, this implies some dequeue completes.

The other possibility is that $deq$ returns EMPTY in each CRQ node $q$ it enters but never reaches the LCRQ’s tail. Each node $q_i$ contains at least one item, and so there is a dequeue $d_i$ that holds the index to this item. After traversing through $T$ nodes, where $T$ is the number of threads in the system, it must be that $d_i = d_j$ for some $j > i$. This means $d_i$ completes and returns. Overall, we have shown that a dequeue must complete within a finite number of steps by dequeuing threads.

**5. Evaluation**

**Evaluated algorithms**  We compare LCRQ to the best performing queues reported in the recent literature, all of which are based on the combining principle: Hendler et al.’s FC queue [11] and Fatourou and Kallimanis’ CC-Queue and H-Queue [7]. We also test Michael and Scott’s classic nonblocking MS queue [19].

The FC queue is based on flat combining, in which a thread becomes a combiner by acquiring a global lock, and then applies the operations of the non-combining threads. The queue we test is a linked list of cyclic arrays, with a new tail array allocated when the old tail fills.

The CC-Queue replaces each of the two locks in Michael and Scott’s two-lock queue [19], which serialize accesses to the queue’s head and tail, with an instance of the CC-Synch universal construction. The CC-Synch universal construction maintains a linked list to which threads add themselves using SWAP. The thread at the head of the list traverses the list and performs the requests of waiting threads. Since the enqueue and dequeue CC-Synch instances work in parallel, the CC-Queue outperforms the FC queue [7].

The H-Queue is a hierarchical version of the CC-Queue. It uses an instance of the H-Synch universal construction to replace the two-lock queue’s locks. The H-Synch construction consists of one instance of CC-Synch per cluster and a lock that synchronizes the CC-Synch instances. Each CC-Synch combiner acquires the lock and performs the operations of the threads on its cluster.

To obtain the most meaningful results, we use the queue implementations from Fatourou and Kallimanis’ benchmark framework [7,8], all of which are in C [5]. We incorporate the FC queue implementation into this framework.

**LCRQ implementation**  We use CRQs whose ring size, $R$, is $2^{17}$. (We include a sensitivity study of LCRQ to the ring size below.) In addition to baseline LCRQ, we also evaluate LCRQ+H, in which we enable our hierarchical optimization (with a timeout of 100 µs). To explore the impact of CAS failures, we test LCRQ-CAS, a version of LCRQ in which we implement the F&As using a CAS loop. All LCRQ variants include the overhead of pointing a hazard pointer at the CRQ before accessing it [5].

**Methodology**  We follow the testing methodology of prior work [7,19]. We measure the time it takes for every thread to execute $10^7$ pairs of enqueue and dequeue operations, averaged over 10 runs. As in prior work, in every test we avoid artificial long run scenarios [19], in which a thread zooms through many consecutive operations, by having each thread wait for a random number of nanoseconds (up to 100) between operations. Each thread is pinned to a specific hardware thread, to avoid interference from the operating system scheduler. Our tests use the jemalloc [6] memory allocator to prevent memory allocation from being a bottleneck. Results’ variance is negligible (we use a dedicated test machine).

**Platform**  We use a Fujitsu PRIMEergy RX600 S6 server with four Intel Xeon E7-4870 (Westmere EX) processors, which were launched by Intel in early 2011. Each processor has 10 2.40 GHz cores, each of which multiplexes 2 hardware threads, so in total our system supports 80 hardware threads. Each core has private write-back L1 and L2 caches; an inclusive L3 cache is shared by all cores.

**Single processor executions (Figure 6a)**  Here we restrict threads to run on one of the server’s processors. This evaluates the queues in a modern multicore environment in which all synchronization is handled on-chip and thus has low cost. We omit results of LCRQ+H and H-Queue, since they are relevant only for multi-processor executions.

LCRQ outperforms all other queues beyond 2 threads. From 10 threads onwards, LCRQ outperforms CC-Queue by 1.5x, the FC queue by $> 2.5x$, and the MS queue by $> 3x$. LCRQ-CAS matches LCRQ’s performance up to 4 threads, but at that point its performance levels off. Subsequently, LCRQ-CAS exhibits the throughput “meltdown” associated with highly contended hot spots. Its throughput at maximum concurrency is 33% lower than its peak performance at 8 threads. Similarly, MS queue’s performance peaks at 2 threads and degrades as concurrency increases.

Table 3 explains the above results. LCRQ, LCRQ-CAS and the MS queue all complete in a few instructions, but some of these instructions.
are expensive atomic operations on contended locations. LCRQ-CAS and the MS queue suffer from CAS failures, which also lead to more cache misses as the algorithm wastes work. In the combining algorithms, communication between combiners and waiting threads causes more cache misses compared to LCRQ.

**Oversubscribed workloads (Figure 6b)** Problems related to blocking usually occur in oversubscribed scenarios, in which the number of software threads exceeds the hardware supported level and forces the operating system to context switch between threads. If a thread holding a lock is scheduled out, the algorithm cannot make progress until it runs again. We show this by increasing the number of threads in a single processor execution beyond 20. The throughput of the lock-based combining algorithms plummets, with FC queue dropping by 40× and CC-Queue by 15×, whereas both LCRQ and the MS queue maintain their peak throughput. As a result, LCRQ outperforms the CC-Queue by 20×.

**Four processor executions (Figure 7)** To measure the effect of the increased synchronization cost between processors, we pin the threads across the processors in a round-robin manner, so that the cross-processor cache coherency cost always exists. One can see how, in contrast to the single processor experiment, when going from 1 to 2 threads the throughput of all algorithms drops due to cross-processor synchronization, except for LCRQ and LCRQ+H.

Figure 7a shows the results when the queue is initially filled with $2^{16}$ elements, thus keeping the queue’s head and tail apart. This causes the throughput of CC-Queue to degrade by $\approx 10\%$ compared to the initially empty case (Figure 7b), due to reduced locality: in an initially empty queue, the queue’s state keeps hovering around empty and so there is a 1 in 4 chance that dequeued items will have just been enqueued on the same processor by the enqueuing combiner. In contrast, switching to an initially filled queue improves LCRQ’s throughput by $\approx 5\%$. The reason is that when the queue is not empty an LCRQ dequeuer does not wait for an enqueuer to arrive at its ring node. (Table 3 shows that LCRQ operations take less instructions to complete.) The reduced locality does not hurt LCRQ because dequeued items are fetched in parallel by all operations, and not sequentially by a single combiner. Overall, using an initially filled queue increases LCRQ’s advantage over CC-Queue from $\approx 1.5\times$ to $\approx 1.8\times$.

Heavy synchronization cost due to lack of locality also explains why only the hierarchical LCRQ+H and H-Queue scale past 16 threads. These algorithms amortize the synchronization cost by running batches of operations on a single processor while operations on other processors wait. However, H-Queue suffers much more from the reduced locality caused when switching to an initially filled queue: it triples the number of L3 misses (Table 3), which must be satisfied from off-chip resources and so its throughput drops by $\approx 40\%$. In contrast, LCRQ+H maintains its performance, increasing its advantage over H-Queue from $1.5\times$ to $2.5\times$. 

**Latency of operations (Figure 8)** Examining the latency distribution of queue operations at maximum concurrency provides more refined insight on the performance of the algorithms. For instance, while the average latency of an LCRQ+H operation is 2.19 $\mu$s (Table 3), 80% of the operations complete in $\leq 0.5\mu$s and 97% in $\leq 2\mu$s. The remaining operations are those that complete only

---

**Table 2:** Single processor average per-operation statistics. Latency numbers are relative to LCRQ. There are no L3 misses because the workload fits into the shared L3 cache.

<table>
<thead>
<tr>
<th>Single processor execution (queue initially empty)</th>
<th>1 thread</th>
<th>20 threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCRQ</td>
<td>LCRQ-CAS</td>
<td>CC-Queue</td>
</tr>
<tr>
<td>Latency</td>
<td>0.13 $\mu$s</td>
<td>0.96 $\times$</td>
</tr>
<tr>
<td>Instructions</td>
<td>278.46</td>
<td>284.96</td>
</tr>
<tr>
<td>Atomic operations</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>L1 misses</td>
<td>0.51</td>
<td>0.51</td>
</tr>
<tr>
<td>L2 misses</td>
<td>0.05</td>
<td>0.06</td>
</tr>
</tbody>
</table>

---

7On a single processor this test yields similar results to an initially empty queue and so we did not discuss it earlier.
Figure 7: Enqueue/dequeue throughput on four processors (threads run on all processors from the start).

Table 3: Four processor average per-operation statistics.

<table>
<thead>
<tr>
<th></th>
<th>LCRQ+H</th>
<th>LCRQ</th>
<th>LCRQ-CAS</th>
<th>H-Queue</th>
<th>CC-Queue</th>
<th>LCRQ+H</th>
<th>LCRQ</th>
<th>LCRQ-CAS</th>
<th>H-Queue</th>
<th>CC-Queue</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency (µs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instructions</td>
<td>1456.65</td>
<td>307.15</td>
<td>338.98</td>
<td>5670.17</td>
<td>16249.94</td>
<td>2151.60</td>
<td>278.62</td>
<td>293.86</td>
<td>9173.94</td>
<td>18224.62</td>
</tr>
<tr>
<td>Atomic operations</td>
<td>2</td>
<td>2</td>
<td>2.88</td>
<td>1.05</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.95</td>
<td>1.05</td>
<td>1</td>
</tr>
<tr>
<td>L1 misses</td>
<td>4.12</td>
<td>2.91</td>
<td>4.15</td>
<td>9.99</td>
<td>10.70</td>
<td>3.43</td>
<td>3.01</td>
<td>4.31</td>
<td>10.60</td>
<td>11.33</td>
</tr>
<tr>
<td>L2 misses</td>
<td>4.15</td>
<td>2.83</td>
<td>4.01</td>
<td>7.10</td>
<td>8.65</td>
<td>3.54</td>
<td>2.90</td>
<td>4.17</td>
<td>7.74</td>
<td>9.07</td>
</tr>
<tr>
<td>L3 misses</td>
<td>0.51</td>
<td>1.47</td>
<td>2.23</td>
<td>0.34</td>
<td>5.90</td>
<td>0.81</td>
<td>1.43</td>
<td>2.22</td>
<td>0.95</td>
<td>6.19</td>
</tr>
</tbody>
</table>

After the timeout expires. The spinning these operations do while waiting accounts for the increased average instruction count of LCRQ+H compared to LCRQ shown in Table 3. In general, LCRQ operations have better latency than combining-based operations, which spend time either servicing other threads or waiting for the combiner. On a single processor, 42% of LCRQ operations finish in ≤ 0.24 µs while none of the combining operations do. On four processors, 80% of LCRQ operations finish in ≤ 9.6 µs compared to 50% of CC-Queue operations. Similarly, 80% of LCRQ+H operation finish in ≤ 0.5 µs compared to 30% of H-Queue operations.

Ring size sensitivity study (Figure 9) The ring size plays an important role in the performance of LCRQ. Intuitively, as the ring size decreases an LCRQ operation needs more tries before it succeeds in performing an enqueue/dequeue transition.

To quantify this effect, we test LCRQ on an initially empty queue at maximum concurrency with various ring sizes. On a single processor, taking R ≥ 32 is enough for LCRQ to outperform the CC-Queue by 1.33×. As R increases LCRQ’s throughput increases up to ≈ 1.5× that of the CC-Queue. In other words, as long as an individual CRQ has room for all running threads, LCRQ obtains excellent performance.

On the four processor benchmark the results are similar, but due to the higher concurrency level, LCRQ outperforms CC-Queue starting with R = 128 and the advantage becomes ≈ 1.5× starting with R = 1024. LCRQ+H requires R = 512 to match H-Queue and R = 4096 to outperform H-Queue by 1.5×.

6. Conclusion

We have presented LCRQ, a concurrent nonblocking linearizable FIFO queue that outperforms prior combining-based queue implementations by 1.5× to more than 2× in all concurrency levels on an x86 server with four multicore processors. LCRQ uses contended F&A objects to spread threads around items in the queue, allowing them to complete in parallel. Because the hardware guarantees that every F&A succeeds, we avoid the costly failures that plague CAS-based algorithms.

Our results show a couple of ways in which modern x86 multicore architecture requires reevaluating conventional wisdom about concurrent programming. First, LCRQ shows that on modern hardware an algorithm with a contended hot spot can scale quite well. Instead, it is CAS retries that are often the cause for notorious “contention meltdowns.” Second, the conventional wisdom in the literature, of avoiding F&A or CAS2 since they are not widely supported, is outdated. We believe these principles can guide the design of future concurrent algorithms.

More practically, the LCRQ algorithm is simple to implement and offers excellent and robust performance on one of today’s dominant multicore architecture. We therefore hope it gets adopted and used in practice.

Acknowledgments

Mike Dodds, Andreas Haas, and Christoph Kirsch, and Joe Israelevitz and Michael Scott discovered that the proceedings version of this paper – which did not include Lines 145–147 in Figure 5 – could lose enqueued items. Vlad Roubtsov pointed out misprints in Figure 3.

This work was supported by the Israel Science Foundation (grant 1386/11), by the Israeli Centers of Research Excellence (ICORE) program (Center 4/11), and by Intel’s lab support program.
Figure 8: Cumulative distribution of queue operation latency at maximum concurrency.

Figure 9: Impact of ring size on LCRQ throughput (CC-Queue and H-Queue results are shown for reference).

References