Openings at the IBM R&D Labs in Israel

Verification Student

Location: Haifa

Description:
This position involves responsibility for planning and coding the major part of a verification testbench in C++, Vera, or system Verilog and developing a formal verification environment

Requirements:
Skills in object-oriented programming (C++/e/System Verilog) is required.
Knowledge in logic design is required.
Skills in PERL, CSH, or KSH programming are an advantage.
Knowledge in verification methodology and tools is an advantage.
Knowledge in communication, IO, memory, and processors IP is an advantage.

Education:
2nd year of computer science or computer engineering or Electrical engineering with enhanced SW track

Apply online!

Position number: STG-0372602

Contact details: Iris Golan- 04-8296292, Efrat Barnea- 04-8296205
Openings at the IBM R&D Labs in Israel

Digital Circuit Design Engineer

**Location:** Haifa or Tel Aviv

**Description:**
This position involves participation in the design of a high-performance circuits for variety systems and CPU. The selected candidate will work with logic design teams to define a block and take it from RTL, draw schematics, and optimize above the CMOS schematic to meet macro design guideline targets. The candidate will perform feasibility spice simulations; create, debug, and optimize the layout; and perform the necessary backend checks.

**Requirements:**
Knowledge in Digital CMOS circuits, as well as reasonable familiarity with CPU/SOC micro-architecture is required.
Advantages: familiarity with custom EDA tools (Cadence schematic and layout tools), previous design experience, custom methodology development, RTL coding, and SRAM/Cache design, scripting skills (SKILL/PERL/TCL)

**Education:**
3rd year Electrical engineering or computer engineering or 1st year

Apply on line!

**Position number:** STG- 0372604

Contact details: Iris Golan- 04-8296292, Efrat Barnea- 04-8296205